A CMOS micropower input amplifier for hearing aids

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This paper describes a CMOS input amplifier for integrated circuits in hearing aids. It has a differential-input differential-output topology, which allows direct driving of cascaded fully-differential processing stages. The adoption of the voltage-to-current conversion and current feedback technique in the amplifying structure, together with the use of a simple differential stage in the offset reduction and in the common-mode feedback loops, allows micropower consumption to be achieved. Experimental results show very good noise and total harmonic distortion performance. Copyright © 1996 Elsevier Science Ltd.

1. Introduction

The input amplifier is a very important element in a signal processing chain. Its task is to increase the input signal amplitude up to a level which can easily be processed by the following stages. The value of the amplifier gain is chosen as a function of the maximum input signal amplitude and the maximum swing allowed by the cascaded stages, and is usually achieved by suitably setting the ratio between two or more passive components, typically resistors.

Low-noise characteristics are required of the input amplifier, to avoid degrading the overall noise performance of the processing chain. For low-power applications, an additional key specification for input amplifiers is micropower consumption. This requirement is particularly stringent in applications where the input section is continuously active, while other sections are disabled as long as no appreciable input signal is present, thus limiting system power consumption to a minimum. In applications such as hearing aids or implantable medical systems, very low power consumption is also desirable so that the amplifier can be powered by a fully-integrated voltage multiplier which generates the required supply voltage from a single low-voltage battery (e.g. 1.3 or 1.5 V) [1, 2]. Moreover, reduced offset must be ensured in input amplifiers, especially when high gain is required, to avoid driving the amplifier output out of its correct operating conditions. CMOS technology is the preferred choice for implementation, as it allows the designer to integrate the amplifier together with all the
required processing functions in a single chip at low cost.

This paper presents a fully CMOS micropower input amplifier specifically designed for integrated circuits for hearing-aid applications. Target requirements are a gain of about 40 dB in the bandwidth from several Hz to ~10 kHz with a maximum input peak signal of 5 mV, low supply voltage ($V_{DD} = 3$ V), micropower consumption ($\leq 50$ $\mu$W) and reduced noise (input referred noise less than 15 $\mu$V$_{rms}$ in the signal bandwidth). The amplifier described exploits the current feedback technique to drive the gain-setting resistors without needing heavy power consumption, and uses large-area input transistors operating in weak-inversion to achieve the noise performance required. The circuit diagram and the operation of the amplifier are discussed in Section 2, and the results obtained by experimental evaluation are presented in Section 3. Very good performance is obtained in terms of noise, power consumption and total harmonic distortion.

2. Circuit description

The operating principle of the proposed amplifier is illustrated in Fig. 1. The circuit has a differential-input differential-output topology, and was designed following the voltage-to-current conversion and current feedback technique [3–5]. Two source followers ($M_1$ and $M_2$) apply the input signal ($v_{in+} - v_{in-}$) across the resistor $R_2$, thus giving rise to a signal current $i_s = (v_{in+} - v_{in-})/R_2$. This current is injected, via common-gate transistors $M_5$ and $M_6$, into the output parallel group ($R_1$, $C_1$). In first approximation, the voltage gain $A(s) = (v_{out+} - v_{out-})/(v_{in+} - v_{in-})$ in the frequency band of interest is given by

$$A(s) = \frac{R_1}{R_2} \frac{1}{1 + sC_1 R_1} \quad (1)$$

The mid-frequency gain $R_1/R_2$ and the low-pass cut-off frequency $f_1 = 1/(2\pi R_1 C_1)$ can be set to the desired values by appropriately choosing passive elements $R_1$, $R_2$ and $C_1$. An output common-mode feedback loop and an offset reduction loop are also provided, as shown in detail in the following subsections. These loops

![Fig. 1. Simplified circuit diagram of the proposed input amplifier.](image-url)
each only include a simple differential stage as an active element ($A_{CM}$ and $A_{OR}$, respectively), thus limiting power overhead.

The differential topology of the amplifier ensures better performance and allows the cascaded stages to carry out differential processing of the output signal with no need for additional single-ended to double-ended conversion structures. Moreover, a low supply voltage can be used thanks to the folded architecture.

The amplifier will now be described in detail, referring to the complete circuit diagram shown in Fig. 2.

2.1 Amplifying stage
The need for low-power operation leads to a problem due to the low transconductance of the input transistors $M_1$ and $M_2$. Its value would oblige us to use a very large resistor $R_2$ in order to minimize the voltage loss in the input structure which, in turn, would lead to an impractical value for $R_1$. This drawback was overcome when implementing the circuit by using two local feedback loops ($A_1$, $M_1$ and $A_2$, $M_2$) that reduce the output impedance of the input source followers. This was obtained with a minor increase in power consumption, noise and silicon area occupation. Amplifiers $A_1$ and $A_2$ are simple differential stages (nominal dc gain = 38 dB). To achieve good noise performance while limiting extra power consumption, the input differential pairs of $A_1$ and $A_2$ were implemented with large-area p-channel transistors [6–10] working in weak inversion [11, 12]. These were laid out with an interdigitized topology to minimize input offset.

To obtain the required mid-frequency gain (~40 dB), the ratio $R_1/R_2$ was set to 100. The nominal values of $R_1$ and $R_2$ were set to 1 MΩ and 10 kΩ, respectively. The output impedance of transistors $MB_3$ and $MB_4$ is of the order of a few megohm, and therefore some gain reduction is to be expected. The desired cut-off frequency ($f_{H1}$ in the range of 10 kHz) was obtained by setting $C_1 = 16 \text{ pF}$. It should be noted that the structure lends itself to easy gain programmability by allowing the value of $R_2$ to be set via digital control [5].

2.2 Output common-mode feedback loop
The output resistor $R_1$ was divided into two equal parts to allow the output common-mode voltage $V_{CM}$ to be detected [13]. A simple differential stage ($A_{CM}$) senses the difference between $V_{CM}$ and the required reference voltage $V_{R,CM}$ (in our design $V_{R,CM} = V_{DD}/2$) and controls the bias current sources at the bottom of the input structure of the amplifying stage ($M_3$, $M_4$), thereby closing the feedback loop and stabilizing the output common-mode voltage. No high-impedance pole is introduced by this loop, thus ensuring its frequency stability.

2.3 Offset reduction loop
The relatively high gain of the amplifier (~40 dB) could lead a small input offset to cause a large dc unbalance in the output stage and consequently drive the circuit out of its correct bias conditions. Therefore, we introduced an offset reduction loop. The differential output ($v_{\text{out}+} - v_{\text{out}-}$) is sensed by a low-gain differential stage ($A_{OR}$) and, after low-pass filtering by the $R_{OR}$-$C_{OR}$ group ($C_{OR}$ external), it controls the current drawn from the output node OUT by transistor $M_{OR}$, thereby closing the feedback loop. As the low-frequency voltage gain of the amplifier is reduced, the offset contribution is limited. If the dc input voltages of the offset reduction amplifier $A_{OR}$ are equal, the current drawn by $M_{OR}$, which mirrors the current through $MR_3$, equals $I_{MR3}/2$. This current is compensated by the additional current source $M_{ADD}$ which injects $I_{MR3}/2$ into the output node OUT. It should be noted that this circuit, which reduces both positive and negative offset, allows us to use only one external capacitor.

The nominal bias current through $MB_1$ and $MB_2$, $I_{RUN}$, must ensure that the input stage is correctly operated even in the presence of the
Fig. 2. Complete circuit diagram of the amplifier.
maximum input offset \( v_{\text{in}} \). To this end, we must set

\[ I_{\text{IN}} > \frac{v_{\text{in,M}} + v_{\text{in,n}}}{R_2} \]  

(2)

where \( v_{\text{in}} \) is the maximum input signal voltage.

2.4 Overall transfer function

At first approximation (i.e., assuming unity voltage gain of the input source followers, infinite output impedance of \( M_{B1}, M_{B2}, M_1 \) to \( M_\alpha, M_{ADD} \) and \( M_{OR} \) and neglecting high-frequency poles), the transfer function of the whole amplifier is given by

\[ A(s) = \frac{R_1}{R_2} \cdot \frac{s^2(C_{OR}R_1R_{OR}) + s(C_{OR}R_{OR} + g_{mOR}A_0R_1)}{s^2 + 1 + sR_{OR}C_{OR}} \]  

(3)

where \( A_0 = \frac{1}{2} \left( \frac{g_mR_1}{g_mR_3} \right) \) is the dc gain of the differential stage of the offset reduction loop \( A_{OR} \) (\( g_mR_1 \) and \( g_mR_3 \) are the transconductances of transistors \( MR_1, MR_3 \) and \( M_{OR} \), respectively). When obtaining eq. (3), we assumed \( R_{OR}C_{OR} \gg R_1C_1 \) and \( g_mA_0R_1R_3 \gg 1 \).

In addition to the pole located at \( \omega_1 \approx 1/\sqrt{R_1C_1} \), the transfer function presents a zero at \( \omega_2 = 1/(R_0C_{OR}) \) and another pole at \( \omega_3 = 1/(R_1A_0g_mR_{OR}/(R_{OR}C_{OR})) \), introduced by the offset reduction loop. To push the effects of this loop below the frequency bandwidth of interest, we used a high-value integrated resistor \( R_{OR} \) (several megohms), and an external capacitor \( C_{OR} \) (few tens of nanofarads).

From eq. (3), the dc gain is equal to \( (R_1/R_2) \cdot (1/g_{mOR}A_0R_1) \), and therefore we have an equivalent offset reduction factor of \( g_{mOR}A_0R_1 \).

In the amplifier described, this was set equal to \( \approx 20 \) dB, which is satisfactory for our application.

3. Integration and experimental results

The amplifier described was integrated with a conventional double-poly-silicon double-metal n-well 2-\( \mu \)m CMOS process (nominal threshold voltages \( \approx 0.6 \) V). The chip microphotograph is shown in Fig. 3.

Resistors \( R_1 \) and \( R_2 \) were implemented by using the n-well layer. Resistor non-linearities are strongly reduced by the differential topology used. Capacitor \( C_1 \) was implemented by using the two polysilicon layers made available by the fabrication process. Resistor \( R_{OR} \) was also implemented in the n-well layer.

The experimental evaluation of the amplifier was carried out by setting \( V_{\text{DD}} = 3 \) V and \( I_{\text{B,R}} \) (bias current source) \( \approx 1 \) \( \mu \)A, resulting in an overall power consumption of \( \approx 50 \) \( \mu \)W.

The measured frequency response is shown in Fig. 4 (\( C_{OR} = 30 \) nF). As expected, the mid-frequency gain is somewhat smaller than 40 dB \( (A = 38 \mathrm{~dB}) \). The low-pass cut-off frequency \( f_1 \) is 8.2 kHz. The high-pass cut-off frequency \( f_0 \) is \( \approx 1.5 \) Hz; it is easily adjusted by changing the value of \( C_{OR} \).

The mean value and the standard deviation of the output offset measured on nine samples were 8.8 mV and 16.4 mV, respectively, which correspond to equivalent input-referred values of 110 mV and 205 mV.

The output spectrum measured in response to a 6-mVp, 1-kHz input sine wave is shown in Fig. 5 (output differential peak voltage = 480 mV). Given the differential topology of the amplifier, even-order non-linearities are strongly reduced, and the third harmonic is dominant. Total harmonic distortion (THD) is \( \approx 47 \) dB. With a 5-mVp input sine wave, the THD is reduced to less than \( \approx 50 \) dB.

The noise performance of the amplifier is illustrated in Fig. 6, which shows the measured
output spectrum when zero input signal is applied. Flicker noise is dominant in the signal bandwidth. The output noise integrated in the frequency band from 5 Hz to 8.2 kHz is equal to \( \sim 920 \mu V_{\text{rms}} \) which corresponds to an input-referred noise of 11.5 \( \mu V_{\text{rms}} \). The noise efficiency factor (NEF) was introduced in [5] to allow the noise-power performance of different amplifiers to be compared:

\[
\text{NEF} = \frac{v_{n,\text{rms}}}{\sqrt{\frac{2}{\pi} \cdot V_{T} \cdot 4kT \cdot BW}}
\]

where \( v_{n,\text{rms}} \) is the input-referred noise rms voltage, \( I_{\text{tot}} \) is the total current drain, \( V_{T} \) is the
operated with $I_{BR} = 0.5 \mu A$ (overall power consumption = 25 $\mu W$ at $V_{DD} = 3 V$), the THD showed only a slight increase, while the total input-referred noise in the signal bandwidth was $\sim 14 \mu V_{rms}$.

4. Conclusion

A fully CMOS amplifier to be used in integrated circuits for hearing-aid equipment has been presented. The circuit was designed to achieve both micropower consumption and low-noise performance. The experimental evaluation showed an excellent noise efficiency factor together with very good total harmonic distortion performance.

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