Low-voltage CMOS four-quadrant analogue multiplier for RF applications

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A CMOS four-quadrant multiplier consisting of four MOS transistors operating in the saturation region is introduced. The circuit exploits the quadratic relation between the current and voltage of the MOS transistor in saturation. Simulation results show that, for a supply voltage of 1.2V, multiplication can be performed at a frequency of 1.8GHz, achieving better performances than a recently proposed similar architecture.

Introduction: In recent years research has been carried out into the development of low-voltage CMOS RF mixers [1–3]. These mixers have good performances but their use for wireless applications is limited by the relatively high bias voltage required. In two recent papers [4, 5], a circuit solution was proposed to achieve a low voltage analogue multiplier, using a cascade of so called ‘combines’. Each combiner is made up of two MOS transistors injecting their current into a load resistor. The series of combiners required to achieve analogue multiplication is shown in Fig. 1. The given structure permits the cancellation of all the linear and quadratic terms produced at the output of each combiner, so that only the terms containing the multiplication of the two signals $v_1$ and $v_2$ remain at the differential output of the final pair of combiners.

![Fig. 1 Multiplier proposed in [4]](image)

The purpose of this Letter is to propose an alternative solution capable of achieving the same result and with a lower sensitivity to component mismatch. The suggested circuit can also obtain a better gain, requiring a more relaxed amplifier at its input.

![Fig. 2 Schematic diagram of multiplier](image)

Design principle: Fig. 2 shows the schematic diagram of the proposed structure. It is composed of four MOS transistors operating in the saturation region. The current equation for the MOS transistor in saturation is approximated by

$$I_D = K'[(v_1 + v_2 + A)^2 - (v_1 v_2 + v_1 A + v_2 A)]$$  (2)

$$I_{D1} = K'(v_1 - v_2 + A)^2$$

$$I_{D2} = K'[-v_1 + v_2 + A]^2$$

$$I_{D3} = K'[-v_1 + v_2 + A]^2$$

$$I_{D4} = K'[-v_1 + v_2 + A]^2$$

where $K' = K W/L$, $V_o = V_{out} - V_{in}$, and $V_{out}$ is the quiescent $V_{ds}$. Therefore, assuming a perfect match, the differential output voltage is given by

$$V_{out} = R(I_{D1} - I_{D2} - I_{D3} + I_{D4}) = 8K'R'v_1 v_2$$  (6)

which is the required multiplication. By contrast, the output voltage of the multiplier proposed in [4] is

$$V_{out} = [-32R'R'K'K'(V_1 - V_{in})(V_2 - V_{in})]v_1 v_2$$  (7)

where $K' = K W/L (i = a, b, c)$.

Comparing eqns. 6 and 7, we observe that the gain of the solutions under discussion is controlled by their DC biasing. In particular the gain depends on the ratio $\alpha = I_{D4}/I_{out}$, being the quiescent current in each transistor and $I_{out}$ the transistor’s quiescent overdrive. Specifically, the gain is proportional to the cube of $\alpha$ for the circuit in Fig. 1 and is directly proportional to $\alpha$ for the circuit in Fig. 2. To achieve a high gain (that optimises the SNR of the multiplier) a value of $\alpha$ as high as possible must be used; therefore, the quiescent overdrive $V_{out}$ should be high compared to the drop voltage $I_{ds} R$. For the circuit in Fig. 1 this rule cannot be fulfilled for low voltage applications. The restriction comes from the following observation: the output of the first four combiners cannot become lower than the threshold of the transistors, otherwise the transistors of the remaining two move into the sub-threshold region and the combiners will not work properly. Now, assuming a swing of the input signal equal to just 0.5 of $V_{ds}$, the maximum current in each transistor becomes 2.25 times the quiescent current. Therefore, in the worst case, the current in $R_1$ (or $R_2$–$R_4$) becomes 4.5 times $I_{ds}$. The following condition results:

$$4.5 I_{ds} R < V_{dd} - V_{in}$$  (8)

Therefore, using for example $V_{ds} = 1.2V$ and $V_{in} = 0.75V$, the drop voltage $I_{ds} R$ cannot exceed 0.1V. The overdrive used must be larger than the input swing (for example by 0.3V), thus $\alpha$ becomes an attenuation factor. It holds 1/3 for the used values and, because of the cubic relationship on $\alpha$, the gain of the circuit proposed in [4] is lower than our solution by a factor of 9.

Non-ideal effects: The multiplication function results from the assumption of a perfect square-law MOS characteristic and fully matched devices. Any deviation from the above conditions produces harmonic components in the output response. Mobility degradation and mismatches in the dimensions of transistors or resistors can be accounted for by the use of a global non-ideality parameter (1+e) in the second term of eqn. 1. For simplicity we assume that the various non-ideality errors $e$ affecting the transistors of the multiplier are uncorrelated. Their contributions are superimposed quadratically and eqn. 7 becomes

$$V_{out} = 8K'R'v_1 v_2 + 4eK'R'v_1^2 + v_2^2 + A^2 + 2(v_1 v_2 + v_1 A + v_2 A)$$  (9)

Therefore, the output contains only four spur extra terms: two linear and two quadratic. In addition we have a random offset. Actually the output is also affected by the nonlinear contribution of the pre-processing required to add and subtract $v_1$ and $v_2$; however, these linear operations can be easily achieved with a suitably high linearity.

Carrying out a similar analysis for the circuit in Fig. 1 we obtain a large number of terms (more than 250); some of them are
responsible for an offset while the rest cause a harmonic spur up to a power of 4 of the input voltages. Considered globally, the contribution of harmonic spurs has a normalised weight equal to \(\sqrt{2}\) that is 3 times larger (10dB) than in our proposed circuit, leading to a worse SFDR (spur free dynamic range).

Simulation results: The circuit in Fig. 2 has been simulated using a standard CMOS 0.5\mu m process. The width-to-length ratios of all transistors is 1200:8. The output currents are converted to a differential voltage through the connection of two 300\Omega resistors. All simulations were performed with a supply voltage of 1.2V and an input sine wave with amplitude \(\pm 250\text{mV}\), and frequency lower than 2GHz. The achieved gain with a perfect matching of components is 2dB for \(f_1 = 1.8\text{GHz}\) and \(f_2 = 1.9\text{GHz}\).

Fig. 3 Simulated spectrum of differential output

The spectrum in Fig. 3 shows that the third harmonic component has an amplitude which is 45dB below the fundamental. A mismatch of 0.2% standard deviation leads to additional harmonic terms but the SFDR worsens by only 2dB. In contrast the circuit in Fig. 1 gives an SFDR of 42dB and with 0.2% of mismatch the SFDR becomes 36dB.

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References


Alternative to Gabor's representation of plane aperture radiation

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An exact procedure based on frame discretisation is proposed as an alternative for overcoming the inherent limitations of the well-known Gabor expansion. Numerical comparisons of these two phase-space methods are presented in the context of aperture radiation to demonstrate the stability, efficiency and accuracy of the frame decomposition, thereby emphasising its advantages over the Gabor representation.

Introduction: In the context of multilector and large aperture antennas, conventional methods, such as physical optics and aperture integral techniques, become prohibitively time-consuming. In such a context, Gaussian beam-mode decompositions do not provide an accurate alternative, since the paraxial approximation is generally not valid and Gaussian beam modes cannot be tracked with simple formulas through successive reflections by arbitrarily shaped reflectors. Hence, discrete phase-space methods [1, 2] have been proposed as an efficient alternative, especially at high frequencies. These methods represent fields as discrete and finite superpositions of elementary Gaussian beams that can be tracked easily in a complicated environment. However, the method usually proposed to discretise fields, the so-called Gabor representation, has recently been shown to be numerically unstable [3]. In this Letter, we propose the use of a frame based representation [3], instead of the Gabor expansion. First, the principle of those phase-space methods is briefly reviewed. Then numerical results are given to compare the frame based decomposition and the Gabor representation.

Fig. 1 Geometrical configuration and beam fields \(B_m\)

Principle: The principle of phase-space methods is outlined for the case of plane aperture radiation (Fig. 1). For simplicity, we consider the scalar problem in a two-dimensional configuration (y-independent), with \(z = 0\) the aperture plane, but the following work can easily be extended to the 3D and vectorial cases.

The first step is the expansion of the aperture field into a set of elementary functions \(w_m\) which are translated in the spatial and spectral domains:

\[
E(x, 0) = \sum_{m,n} A_{mn} w_{mn}(x) = \sum_{m,n} A_{mn} e^{i(m\Delta x + n\Delta y)}
\]

where \(A_{mn}\) is the coefficient to be determined, \(\Delta x\) and \(\Delta y\) are, respectively, the spatial and spectral shifts. Such an expansion (eqn. 1) is valid if and only if the shift parameters are constrained by the relation \(|k| = 2\pi v\) with \(v < 1\). The Gabor expansion is obtained for \(v = 1\) and \(l = L_u\) whereas for \(v < 1\) the functions \(w_m\) form what is called a frame [3].

From this aperture field decomposition it follows that the radiated field at an arbitrary observation point can be expressed as

\[
E(x, z) = \sum_{m,n} A_{mn} e^{i(m\Delta x + n\Delta y)} B_{mn}(x, z)
\]

where

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