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An Integrated Microsystem for 3-D Magnetic Field Measurements

Piero Malcovati and Franco Maloberti

Abstract—In this paper, we present a portable, battery-operated, three-dimensional magnetic microsystem (magnetodosimeter), intended for monitoring the workers’ exposure to magnetic fields in particular working environments, such as hospitals or physics laboratories. The proposed microsystem is based on a multichip module containing three equal channels for the three components of the magnetic field measurement, a microprocessor, and a memory. Each single-chip channel detects the magnetic field, converts it into the digital domain, and delivers the result to the microprocessor by means of an on-chip serial interface. The single-chip channel, fabricated in a 0.8-μm CMOS technology, is sensitive to magnetic fields ranging from −200 to +200 mT, achieving 12 bits of resolution, 11 bits of linearity, and an overall accuracy better than 1% in the temperature range from −20 to +80 °C.

Index Terms—Analog–digital conversion, CMOS integrated circuits, magnetic field measurement, magnetic transducers, microsensors, sigma–delta modulation.

I. INTRODUCTION

Some working environments, such as hospitals (magnetic resonance) or physics laboratories (nuclear experiments), are polluted by strong low-frequency magnetic fields. In order to guarantee workers’ health and protect employers against legal actions, therefore, it is essential to monitor the integral exposure of each worker to a particular level of field. In order to accomplish this task, inexpensive battery-operated magnetodosimeters such as magnetic field sensitive badges are required. These devices have to monitor the module of the magnetic field vector in the environment during a whole working shift and store a histogram of the magnetic field levels. Moreover, at the end of the working day, the data stored in the magnetodosimeter have to be dumped on a PC.

The level of magnetic field known to be dangerous for human beings can be detected by silicon magnetic sensors fabricated in conventional CMOS technologies, such as Hall devices [1]. It is, therefore, possible to realize at low cost a single chip containing both the magnetic sensor and the interface circuits required to detect a single component of the magnetic field. In this paper, we present an integrated microsystem for magnetic field measurements, specifically designed to be the core of a miniaturized magnetodosimeter. The proposed device detects the magnetic field in the environment, converts it into the digital domain, and delivers the result to a microprocessor by means of an on-chip serial interface.

II. MICROSYSTEM ARCHITECTURE

The most important requirements of the magnetodosimeter and, hence, of the single-chip channel are summarized in Table I. In order to cover the magnetic field range from −200 to 200 mT with steps of 100 mT at least 11 + 1 bits (2048 levels and a sign bit) are required. However, since the sign of the magnetic field is not relevant in this application, only the 11 least significant bits (LSB’s) are stored in the RAM. Hence, the size of the memory required to monitor the magnetic field once per second during a whole working shift is 720 KB (12 bits of data and 4 bits of additional information for 10 h).

Fig. 1 shows the complete magnetodosimeter. The system is based on a multichip module containing three equal channels for the three components of the magnetic field (Bx, By, and Bz), a microprocessor, and a memory.

Each single-chip channel consists of a Hall device with front-end circuitry, an instrumentation amplifier, an incremental analog-to-digital (A/D) converter with the required digital circuitry, and a serial bus interface, which interconnects the three modules with the microprocessor, as shown in Fig. 2(a).

The magnetic sensor used is a spinning current Hall device [2], which produces an output voltage proportional to the magnetic field component perpendicular to the chip with offset lower than 8 μV. The sensitivity of this particular device, equal to 200 μV / (mA mT), can be trimmed by properly setting the bias current (the nominal value is 1 mA), in order to achieve the required accuracy (12 bits) in the whole system [3]. The front-end circuitry includes current sources and switches for implementing the spinning current offset compensation.
technique and a low-pass filter for removing the resulting out-of-band tones.

III. INTERFACE CIRCUIT DESCRIPTION

The signal obtained at the output of the sensor over the considered magnetic field range is of the order of few tens of millivolts, thus requiring low-noise and low-offset amplification before A/D conversion. In order to achieve the required noise and offset performance in CMOS technology, we used chopper stabilization, as shown in Fig. 2(b). The sensor output signal, modulated with a square wave, is shifted in a region of the spectrum where the noise of the instrumentation amplifier and of the A/D converter is dominated by the thermal component. After amplification and A/D conversion, then, the signal (BS) is modulated again in the digital domain and shifted back in the original band.

The offset and the large low-frequency noise of the instrumentation amplifier and the A/D converter (flicker noise) are also modulated and, hence, pushed at high frequency, where they are removed by a subsequent digital low-pass filter (Counter).

A. Instrumentation Amplifier

The schematic of the used high-input-impedance instrumentation amplifier is shown in Fig. 3. The resistive feedback provides a gain of ten ($R_1 = 54 \, k\Omega$ and $R = 12 \, k\Omega$), while the cross-coupled switches connected to the input allow us to implement the chopper stabilization.

The operational amplifiers used in the instrumentation amplifier are based on a folded-cascode structure followed by a p-channel source follower, which drives the resistive feedback, as shown in Fig. 4.

B. Incremental A/D Converter

The output signals of the instrumentation amplifier are directly connected to the input of an incremental A/D converter, which allows high resolution (in this case 12 bits) to be achieved with a simple hardware and a low power consumption.

The schematic of the switched-capacitor incremental A/D converter [4], [5] is shown in Fig. 5, while the capacitance and design parameter values are summarized in Table II. This circuit, consisting of an integrator with autozero [6], a latched comparator, and a flip-flop (D), is very similar to a first-order
Fig. 4. Schematic of the operational amplifier used in the instrumentation amplifier.

Fig. 5. Schematic of the 12-bit incremental A/D converter.

Fig. 6. Schematic of the operational amplifier used in the incremental A/D converter.

Fig. 7. Schematic of the regenerative latched comparator used in the incremental A/D converter.

**Table II**

CAPACITANCE AND PARAMETER VALUES OF THE 12-BIT INCREMENTAL A/D CONVERTER

<table>
<thead>
<tr>
<th>Capacitor</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Integrating Capacitor $C_1$</td>
<td>2 pF</td>
</tr>
<tr>
<td>Input Capacitor $C_{in}$</td>
<td>2 pF</td>
</tr>
<tr>
<td>Reference Capacitor $C_{ref}$</td>
<td>2 pF</td>
</tr>
<tr>
<td>Sample and Hold Capacitor $C_{s}$</td>
<td>2 pF</td>
</tr>
</tbody>
</table>

Clock Frequency, 1 MHz

Sigma–delta modulator. The integrator, however, is reset at the end of each conversion cycle ($\Phi_R$), consisting of $2^N$ clock periods, where $N$ is the required resolution.

Because of the periodic reset of the integrator, the behavior of this circuit is deterministic rather than stochastic (i.e., for equal input signals, we obtain equal output bitstreams). Moreover, the decimating filter can be reduced to a simple up/down counter, as shown in Fig. 2. The incremental conversion algorithm is described by

$$U_{k+1} = U_k + (V_{in} - (-1)^{BS_k}V_{ref})$$

(1)

where $U$ and $BS_k$ denote the output signals of the integrator and the comparator (bitstream), respectively, while $k$ denotes the current clock period, $V_{in} = V_{in,p} - V_{in,n}$ the input signal, and $V_{ref}$ the reference voltage. The $N$-bit digital output signal obtained after $2^N$ clock periods is, therefore, given by

$$Out = \sum_{i=0}^{N-1} BS_i = \text{Round}(2^N \frac{V_{in}}{V_{ref}}).$$

(2)

The operational amplifier used for the integrator is based on a fully differential, folded-cascode structure with switched-capacitor common-mode feedback (CMFB) [7], as shown in Fig. 6. The latched comparator [8], whose schematic is shown in Fig. 7, consists of a p-channel input differential pair ($M_{p1}$ and $M_{n1}$), two bistable regenerative loops ($M_{4}$, $M_{6}$, $M_{8}$, and $M_{10}$), and an output latch ($M_{12}$, $M_{13}$, $M_{15}$). During clock phase $\Phi_R$ (reset phase), the comparator is reset by means of switches $M_{3}$, $M_{11}$, and $M_{7}$. On the falling edge of $\Phi_R$, then, the comparator is latched and, depending on the input signal ($V_{in,p} - V_{in,n}$), the regenerative loops reach one of the two stable states (“one” or “zero”). This state is then maintained by the output latch until the end of the next reset phase, independently of the input signal. Due to the regenerative effect, this comparator allow very fast transients (of the order of 100 ns) and high resolution (around 40 μV) to be achieved.

The incremental A/D converter is operated with a clock frequency of 1 MHz.

C. Digital Section

The digital section of the proposed microsystem consists of a chopper modulator (multiplexer), an up/down counter for decimating the output bitstream ($BS$) of the incremental A/D converter, the logic required for controlling the operation of the
incremental A/D converter, and a serial interface for interconnecting the three channels of the magnetodosimeter with the microprocessor.

The serial interface implements a standard two-wire (data and clock) communication protocol between A/D converters and microprocessors. The microprocessor provides a chip select signal (CS), which enables the A/D converter. After \(2^{N}\) clock cycles, when the data are ready, the A/D converter produces an end-of-conversion signal on the data line. The microprocessor, then, provides a clock signal on the clock line and reads the data serially on the data line.

When the chip is not selected (CS), the whole system enters in power-down mode (the analog blocks, including the sensor are switched off) in order to reduce the average power consumption. In fact, if the magnetic field sampling frequency is set to 1 Hz, the system is operated with a 0.4% duty cycle.

IV. EXPERIMENTAL RESULTS

A prototype of the single-channel chip, whose micrograph is shown in Fig. 8, has been integrated in a standard 0.8-\(\mu\)m double-poly, double-metal CMOS process. The total die area, including pads, is \(3.2 \times 2.1 \text{ mm}^2\). The chip has been characterized by applying a dc magnetic field at the input and acquiring the digital output in a PC.

The measured integral (INL) and differential (DNL) nonlinearities of the whole system are shown in Figs. 9 and 10, respectively. The INL represents the displacement of the static transfer characteristic of the system from the ideal staircase, while the DNL represents the ratio between the real and the ideal quantization steps of the system. The obtained results lead to an effective resolution of 12 bits with 11 bits of linearity (without calibration) for the single component of the magnetic field. The slight degradation in the linearity performance can be corrected digitally by the microprocessor if required, although in the considered application 11 bits of linearity are sufficient. The chopper stabilization effectively reduces the offset of the system below 0.5 LSB.

The communication between the single-channel chip and the microprocessor through the serial interface is completely functional. The overall accuracy of the system after calibration of the sensitivity is better than 1% in the temperature range from \(-20\) to \(+80^\circ\)C. The single-channel chip consumes 41 \(\mu\)W from a 5-V power supply with 1-Hz magnetic field sampling frequency (0.4% duty cycle).

V. CONCLUSIONS

In this paper, we presented a a portable, battery-operated microsystem (magnetodosimeter) sensitive to three-dimensional (3-D) magnetic fields, ranging from \(-200\) to \(+200\) mT. The system is based on a multichip module containing three equal channels for the three components of the magnetic field, a microprocessor, and a memory. Each single-chip channel consists of a spinning current Hall device with front-end circuitry, an instrumentation amplifier, an incremental A/D converter, and a digital section. Chopper stabilization is used to cancel the offset of the system. An on-chip two-wire serial interface allows the communication between the three channels of the magnetodosimeter and the microprocessor. The single-channel chip, fabricated in a 0.8-\(\mu\)m CMOS technology, achieves 12 bits of resolution, 11 bits of linearity, and an overall accuracy better than 1% in the temperature range from \(-20\) to \(+80^\circ\)C.

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