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High-Speed Data Converters for Communication Systems

by Franco Maloberti
Introduction

The tremendous progress in microelectronics significantly benefits the communication area. We are enjoying an unprecedented growth in mobile communication: new services are being constantly introduced thanks to the availability of new integrated circuits and systems. This progress results from two key components: DSP and the data converter. Using sub-submicron technologies it is possible to integrate millions of transistors on a single chip. The speed of digital circuits is increasing up to many hundreds of MHz or even GHz. Hence, new DSP architectures allow complex algorithms to be implemented at very high computation speeds. However, analog-digital interfaces must be able to match the resolution and the speed of the DSP. Therefore, the second key component completing the basic design set is the high speed and high resolution data converter [1].

The present trend pushing the border of digital conversion toward the transmit and receive terminal leads to ever increasing demands on specifications, namely speed and resolution. We will see that often more than 14 bits and several hundreds of MHz are required. In addition, many applications impose continuous reductions in power consumption. As a result, market challenges favor research on high speed data converters. In turn, the results achieved lead to new architectural solutions which create new needs. This paper analyses this process and discusses recent circuit solutions suitable for meeting key system specifications [2].

Communication Systems

It is possible to use three main transmission media for analog communication and for data transfer: wireless, twisted-pair cable and coaxial cable. Optic fibers are also employed, but their high cost makes their use suitable for backbone networks or for central office and optical network unit (ONU) con...
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nections. For data communication, it is possible to utilize either narrow-band connections (up to 56 kb/s) or broadband connections (like the T-1 service operating at 1.544 Mb/s). Around the options of media and bandwidth, communication engineers can build many possible architectures. We shall see that in many of them, data converters have a significant role.

Wireless Telephony

For narrow-band wireless we have different standards around the world. In Europe we have the DCS and GSM operating in two different frequency bands: 900 and 1800MHz (GSM900 and GSM1800). In the USA we have various mobile radio standards in the 1800 MHz frequency band, among them the IS-95 and the IS-136. Moreover, studies on globalization of personal communications begun in 1986 are going to define new standards for the so called 3G (third generation) mobile telecommunication systems. The standards will follow an evolutionary path so as to protect the capital investment done for the second generation standards. Thus, the present scenario is such that, despite the considerable effort spent on harmonization, it will be hard to establish a unique world-wide standard for future mobile radio systems. Consequently, managing multiple standards will be ever more necessary, creating difficulties for both manufacturers and operators.

Significant help can come from the so-called “software radio” approach [3]. Figure 1 shows the “ideal” software radio solution: a high speed data converter digitizes the RF signal directly at the antenna with all radio functions being performed in the digital domain possibly using a specialized reconfigurable hardware. At present (but even in the future) it is impossible to imagine a data converter operating at 1 or 2 GHz and delivering 16-18 bits. Therefore, because of obvious difficulties in the implementation of the “ideal” solution the data converter is moved after some analog preprocessing. This is done typically after the low noise amplifier and a first mixing (Fig. 2b, showing the Rx section). Unlike a conventional Rx architecture (Fig. 2a) the data converter in the software radio (Fig. 2b) runs at the IF frequency and a digital processor performs the IF filtering, the IF mixing, the band-base filtering and the demodulation.

More generally, software radio envisages a base station platform with reconfigurable hardware and software. This architecture can be adapted to different standards or services simply by using the appropriate software. Software radio offers many advantages: it is flexible, allows new services to be added quickly thus shortening the time-to-market, and offers better management of logistics, maintenance and
personnel training. Moreover, software radio permits migration from one standard to the successive generation along an evolutionary path.

About data converters, observe that, because the channel tuning is performed in the digital domain, the linearity of the converter must be such as to avoid any spurious interference. Fortunately the bandwidth licensed to operators is limited, typically in the range 20-40 MHz. Therefore, appropriate choice of the LO frequency and the sampling frequency of data converters allows some system flexibility that can place images and spurious signals out of band. Thus, data converter specifications depend on the architecture and standard adopted. For modern architectures they span from 12 to 16 bit with spurious performances around 100 dB. The sampling frequency ranges from 60 to 100 MHz.

Figure 3 show the Tx section of a typical software radio architecture. It uses, as an example, an 80 MHz clock, thus permitting a 40 MHz bandwidth. Suitable digital-up conversions (DUC) allocate the transmission channels in the selected frequency slot. All the digital channels are converted into analog by a single DAC. The result, after suitable filtering and modulation, drives the power amplifier that, in turn, drives the antenna. Figure 3 indicates some possible design issues: a “sinc” attenuation shapes the spectrum after the DAC; the continuous-time low pass filter in the IF section should carefully remove the frequency components beyond 40 MHz, the RF bandpass filter should take care of the im-
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age rejection. Thus, if the channels occupy almost the 40 MHz available the filters design becomes quite problematic. The insert in the figure shows a possible solution: an interpolator increases the clock frequency by a factor 4 so that a band-pass digital filter can select the first image of the transmission spectrum. Therefore, after the DAC the signal used suffers by a limited sinc attenuation, it is 40 MHz apart from dc and its image falls between 240 and 280 MHz. These features permit a significant relaxation of the filters’ specs. However, the clock frequency of the DAC must be 320 MHz. Thus, more demanding performances on the data converter help us in optimizing the system architectures. Modern CMOS technologies permit achievement of 12 bit DACs with spurious performances around 95 dB and sampling frequency as large as 400 MHz [4].

Smart Antennas

In cellular communication, important features are coverage, capacity and service quality. In rural areas ensuring a proper coverage is expensive; in urban areas the capacity is often close to average demand. Moreover, interference from neighbor cells worsens service quality. Smart antennas provide an answer to these problems [5]. A smart antenna is a directional antenna used in the base station to track mobile terminals (Fig. 4). The basic structure uses a switched-beam or an adaptive array architecture. Two or more antenna elements are spatially arranged and the signals are properly processed to produce a directional radiation pattern.
In its simplest form, a smart antenna uses a fixed phase beam network that is switched to the elements of the array so as to produce a beam close to the desired direction. In the phased array the phases of signals are adjusted to change the array pattern, thus tracking a given mobile or cancelling a given interference signal.

Here, different strategies for rural or urban areas are necessary. Therefore, adaptive and reconfigurable architectures are the best solution. Figure 5 shows the block diagram of a possible “digital” implementation. The architecture uses a weight-adjustment algorithm to obtain IF beam-forming. Of course the given architecture is only one possibility; we could design a solution fully in the analog domain. Nevertheless, the digital approach, thanks to the use of the data converter in the IF section, permits complex beam-forming with a digital processor. Therefore, the availability of data converters which answer system requirements leads us to an adaptive system providing superior performance.

The data converter specifications depend on the IF frequency used. Even for these applications the resolution depends on the width of the bandwidth granted to a given provider. In the case of 10MHz we can satisfy the GSM specifications (receive side) with an 81 dB dynamic range (13.5 bit) and a 97 dB SFDR. Moreover, the clock jitter must be kept below 2 ps. The above figures assume an IF frequency of 70 MHz. More relaxed figures result when considering other standards like the DCS1800.

Broadband Services

Broadband communication offers many examples of architectures that exploit data converters and DSP. Through the already installed copper twisted-pair phone lines it is possible to provide broadband digital services. We have various possibilities, the ADSL (Asymmetric Digital Subscriber Line), HDSL (High Speed), the RADSL (Rate Adaptive) and the VDSL (Very High Speed). The first class runs at a data rate of up to 8 Mb/s in the downstream direction (from the central office to the subscriber) and up to 1 Mb/s in the upstream direction. The distance from the central office to the subscriber, however, must be a maximum of 5 km. The VDSL service is more advanced; it can provide a data rate as high as 52 Mb/s.

The architecture provides a fiber optical connection from the central office to the neighborhood of a group of customers (Optical Network Unit, ONU). The connection from the ONU to the subscriber is through a short link (not more than 1200 m) of twisted-pair copper wire [6].

The above features are made possible by complex modulation schemes and the relatively high bandwidth of twisted-pair wires (much higher than the 3 kHz filtered voiced channel). An example of VDSL architecture is

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shown in Fig. 6 [7]. Note that it includes an A/D and a D/A converter very close to the twisted-pair connection. For the ADSL architecture the sampling rate in the two links is 8–10 MHz and the required resolution is 12-14 bits. For VDSL architectures the resolution required is a bit lower but the sampling rate must be programmable from 1 MHz to 52 MHz.

High Speed Data Converters

All the data converters in the architectures discussed so far require high speed. Table 1 summarizes the key specifications required. Observe that the conversion rate ranges from 10 MHz to 100 MHz. This feature combined with the resolution and the SFDR make the converter feasible in submicron CMOS technology for the ASDL and the VDSL applications. Instead, the higher resolution and the demanding SFDR posed by the GSM and the smart antenna implementations impose significant bandwidth and linearity. Thus, GSM and smart antenna typically demand submicron BiCMOS (silicon or silicon-germanium) technologies. Presently, the $f_T$ of state-of-the-art submicron CMOS (0.12 µm) exceeds 20 GHz while advanced BiCMOS or SiGe permit bandwidths on the order of 60 GHz. Therefore, speed is an issue that can be satisfactorily addressed by exploiting the available technology. In contrast, accuracy depends on the components’ precision and on practical limits related to circuit implementation. Therefore, the processes used, as well as deep-submicron line widths, should

<table>
<thead>
<tr>
<th>Feature</th>
<th>GSM</th>
<th>Smart Antenna</th>
<th>ASDL</th>
<th>VSDL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>14 bit</td>
<td>13.5 bit</td>
<td>12 bit</td>
<td>12 bit</td>
</tr>
<tr>
<td>Conversion Rate</td>
<td>60-100 MHz</td>
<td>40-60 MHz</td>
<td>10 MHz</td>
<td>52 MHz</td>
</tr>
<tr>
<td>Clock Jitter</td>
<td>4 ps</td>
<td>2 ps</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>SFDR</td>
<td>100 dB</td>
<td>95 dB</td>
<td>60 dB</td>
<td>65 dB</td>
</tr>
<tr>
<td>Technology</td>
<td>BiCMOS/SiGe</td>
<td>BiCMOS/SiGe</td>
<td>CMOS</td>
<td>CMOS</td>
</tr>
</tbody>
</table>
also provide precise resistors and capacitors. At this purpose special layout techniques and a careful control of the process are beneficial. These actions are only effective, however, when not more than 10–12 bits are required. For higher resolution the best way to get rid of inaccuracy is to use calibration. Moreover, to avoid SNR degradation, the analog critical nodes must be conveniently protected from spurious signals and noise. This demand imposes additional steps on the process: it is necessary to utilize, for example, multiple diffused wells, trench separation or migrate toward SOI technologies.

**High-Speed A/D Architectures**

The simplest way to achieve high speed is to use one step or two step flash architectures. The techniques have been used extensively in the past; however, various limitations do not allow us to step outside the 10 bit limit [8]. Another approach is the folding and interpolation technique. Folding consists in nonlinear input processing that produces an output characteristic like a triangular wave. The number of foldings performed determines the MSBs (3 bits is a normal figure). Subsequent data conversion determines additional LSBs. Folding is often associated with interpolation: a suitable network processes two folded outputs and produces transition levels intermediate to the one given by the folding transformation. We can thus extract additional bits at a reduced cost. An example of folding and interpolation architecture is given in [9]. The circuit achieves 10 bits and 40 MS/s using a 7 GHz 0.6 µm CMOS technology.

The two step flash and the folding technique don’t permit us to achieve very high accuracy. By contrast a pipeline architecture (when it incorporates digital calibration) can reach 12–14 bits so as to suit speed requirements and low power consumption demands. Because of that designers more and more utilize pipeline based converters for communication needs. Figure 7 shows a typical pipeline scheme. A number of cells compose the structure. Each cell provides a given number of bits at the output (say, \(N\) bits) and a residual voltage. The next cell processes the residual voltage, performs digital conversion and gives another residual voltage. The output of the entire system comes from the bits generated by each stage. Because the dynamic range of the residual voltage is smaller than the input by a factor \(2^N\), many architectures foresee an amplification of the residual voltage by the same factor to keep the dynamic range constant along the pipeline. The residual output of each cell is

\[
V_{i, \text{res}} = \left[ V_{i, \text{in}} - \frac{b_{n,0} + 2b_{n,1} + \ldots + 2^{N-1}b_{n,N-1}}{2^N} V_{\text{Ref}} \right] 2^N
\]

where \(b_{n,i}\) are the bits generated by the \(n\)-th cell. Possible errors come from an inaccurate amplifier and from offsets in the DAC or in the ADC. Offsets are normally corrected digitally. Each stage of the pipeline provides the digital information with some redundancy.
(for a 1 bit per stage architecture, 0.5 additional bit). Redundancy avoids loss of information even in the presence of offsets and permits cancellation of inaccuracies [10], [11].

Designers widely use the sigma delta technique for band-base applications. Recent technology advancements expand the usable bandwidth and extend the applicability of sigma delta converters to medium and high frequency applications (as required by communication architectures). Sigma delta modulators exploit oversampling, that means using a sampling frequency much higher than twice the signal band. Oversampling and a proper shaping of the quantization error spectrum permit us to significantly attenuate the power of the quantization noise in the band of interest [12]. Figure 8 depicts this basic concept. If we increase the sampling frequency of a conventional converter by a factor 2 the power of the quantization noise \( \Delta^2/12 \) (\( \Delta \) is the quantization step, \( V_{\text{ref}}/2^N \)) is spread over a double frequency interval; therefore, the amount of noise power that falls in the band of interest halves. Noise shaping does better: as shown in Fig. 8 the noise in the band of interest is quite low even if we have much more noise outside. Therefore, a digital filter that rejects out the band noise permits us to achieve a pretty good SNR. Remembering that the number of bits, \( n \) and the SNR are related by

\[
\text{SNR} = 6.02 \cdot n - 1.73
\]  

an increase of the SNR leads to more bits of accuracy.

Sigma delta modulators produce noise shaping by including the quantization into a feedback loop. Figure 9 shows the generic configuration of a sigma delta. With a linear model an additive term \( n(z) \) represents the quantization error. Thus, in the circuit we have two inputs: the input signal and the quantization error. The design target is to leave unchanged the signal while shaping the quantization error. By inspection of the circuit we derive the signal transfer function and the quantization-error transfer function

\[
Y(z) = S(z)u(z) + Q(z)n(z)
\]  

\[
S(z) = \frac{H_1(z)}{1 + H_1(z)H_2(z)}
\]  

\[
Q(z) = \frac{1}{1 + H_1(z)H_2(z)}
\]  

A proper choice of the transfer functions \( H_1 \) and \( H_2 \) (we normally set \( H_2 \) to 1) achieves the target. A huge number of papers deal with the definition and the design of modulator architecture. Designers of converters for...
communication systems will take advantage of that huge previous work [12].

**High Speed DAC Architectures**

The limited bandwidth of amplifiers used mainly limits the speed of analog systems. Thus, all the DACs operating at very high clock rate don’t use op-amps or amplifiers. It is possible to achieve digital-to-analog conversion without active elements by using the current steering approach [13]. Equal (or binary ratioed) current sources are properly switched toward the matching resistance or a dummy resistance. Figure 10 shows \(n\)-channel cascode current sources switched by simple differential pairs. More complex architectures can be envisaged. Nevertheless, the technique is quite simple; possible design problems come from current sources matching inaccuracy and the consequent request to use special techniques and achieve mismatch compensation. Moreover, a non-simultaneous switching of current sources produces glitches in the output voltage. This deteriorates the converter performance. Many papers discuss how to face the above mentioned issues. Readers can refer, for example, to [14],[15]. The area consumption of a current steering architecture can be quite small: it is possible to achieve a 10 bits converter in only 0.6 mm\(^2\) [16]. Moreover, it is possible with modern technologies to combine the analog-to-digital conversion and digital processing as outlined in Fig. 3 [17].

**Conclusions**

We have seen that the tremendous pace in telecommunication developments affects (and is produced by) improvements in data converter performance. We have a combination of technological advances and novel architectures. Typically, benefits come from an extensive use of digital correction and calibration. Therefore, we can talk about a new approach for achieving high performance: using “digitally assisted” data converters.

The market already offers data converters running at 80 Mb/s with 14 bit resolutions and a SFDR of 100 dB. The technology used is, in some cases, specifically optimized for the application. Nevertheless, progress in CMOS processes will soon make available 0.15-\(\mu\)m technologies with migration to the 0.12-\(\mu\)m mark by the year 2001. It is expected that 0.09-\(\mu\)m effective channel length will be achieved by 2001 and 0.07-\(\mu\)m by 2004. If these features are combined with a suitable defense from spur interference, 18-bit, 200 Mb/s data converters capable of answering a wide spectrum of telecommunication needs will be on the market by the first decade of the next century.

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*Figure 10. Principle of operation of the current steering DAC.*

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\[ V_{b2} \]

\[ V_{b1} \]
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