A 1 V Second Order Sigma-Delta Modulator

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Abstract. A second order switched capacitor sigma-delta modulator operating at a supply voltage of 1 V is presented. This low supply voltage restricts the gate overdrive voltage available for switching transistors. The design relies on the elimination of critical switches by using a modified switched op amp for the integrator and novel switched half-supply and reference voltage generators. The design has been carried out in a fully differential configuration in order to minimize errors arising from charge injection and clock-feedthrough effects. The converter has been implemented using a conventional 0.8 μm double-poly double-metal CMOS process, having a nominal threshold voltage of 0.75 V. Test results, showing more than 9 bits of resolution with an oversampling ratio of 64, are also presented.

Key Words: low voltage CMOS circuits, SC circuits, sigma-delta modulation

1. Introduction

Sigma-delta modulators are a class of noise-shaping oversampling modulators having a single-bit DAC as quantizer. Although the quantization error of a 1-bit DAC is high, sigma-delta modulators shape the quantizer noise spectrum such that noise power is pushed to higher frequencies: in this way, the quantization noise can be filtered using a digital low-pass filter. Sigma-delta modulators are an ideal choice for low cost CMOS analog-to-digital interfaces, since low precision analog building blocks can be used while still maintaining high resolution via the use of digital post-processing. Sigma-delta modulators are used for audio processing, medical and instrumentation applications [1]. It is desirable to use a low supply voltage in order to reduce the battery size and weight in portable equipment. Another important driving force towards low voltage operation is the reduced gate oxide breakdown voltage of the MOS transistor due to reduced line widths in today's sub-micron technologies [2].

Sigma-delta modulators have been implemented in different topologies, such as third [3,4] and fourth [5,6] order architectures which operate at 5 V. For low voltage applications, the use of a multi-threshold technology [7] and clock boosting [8] techniques have been investigated, while a single-ended configuration operating at 1.5 V has also been designed [9]. In this design,

a second order architecture has been chosen since it offers a good noise-shaping characteristic while still being robust in terms of loop stability and does not require precise circuit matching when compared to higher order modulators [10]. Furthermore, the required digital post-processing involved in low-pass filtering the digital output of the modulator is more complex in higher order systems.

This paper proposes a 1 V sigma-delta modulator based on a modified switched op amp [11] and novel switched reference generators. A major problem encountered in switched capacitor circuits operating at a supply voltage less than twice the threshold voltage, (which is 0.75 V in this case) is the proper operation of transistor switches. The present design solves this problem by ensuring that transistor switches have one terminal connected either to V_{dd} potential (p-MOS transistors) or to ground (n-MOS transistors), thereby eliminating transistor switches in signal paths.

2. Implementation

2.1. System Overview

The sigma-delta modulator has been implemented using the Boser-Wooley [12] architecture with two summing integrators having a gain factor of 0.5. This architecture requires small signal swings at the

Fig. 1. Block diagram for the second order sigma-delta modulator.

outputs of the integrators and thus results in a converter with good dynamic range: this is an important issue for low supply voltage operation. A block diagram of the linearized system is shown in Fig. 1, where C_g and $E(z)$ represent the gain and quantization noise of the comparator. The modulator consists of two switched-capacitor (SC) integrators, having a half-period delay in the forward path, a quantizer based on a clocked comparator and two switched-DACs which are used in the feedback path. The quantizer introduces a further half-period delay. An additional half-period delay required in the feedback path to the first integrator is introduced via the use of positive-edge triggered D-type latches. The z -domain transfer function for the modulator, using the linear model for the quantizer, with C_g equal to 4, is given by:

$$y(z) = z^{-\frac{3}{2}}x(z) + (1 - z^{-1})^2 z^{-\frac{1}{2}} E(z)$$

Hence the input $x(z)$ appears at the output of the modulator with only a delay, while the quantization noise $E(z)$ is shaped by the high-pass function $(1 - z^{-1})^2$.

The comparator and the op amps used for the integrators in Fig. 2 have an n-MOS differential input pair and therefore their common mode input voltage was set to V_{dd} in order to provide sufficient gate overdrive. The corresponding component sizes are shown in Table 1. Capacitors $C1$ – $C10$ provide the necessary level shift from $V_{dd}/2$ to V_{dd} , while $C11$ – $C14$ are the integration capacitors. All switches shown in the diagram are connected either to V_{dd} or to op amp virtual point which is also at V_{dd} potential. Therefore these switches can be easily implemented using p-channel transistors. The circuit is driven by a 2-phase clock generator which

provides the non-overlapping clock phases $K1$, $K2$ together with their complements $nK1$ and $nK2$.

During phase $K1$ the following operations take place:

- (i) capacitors $C1$ and $C2$ are precharged with the input voltage, while $C7$ and $C8$ are precharged with the reference voltage generated by the switched DAC of the first integrator;
- (ii) voltage generators $V_{dd}/2\text{Gen}$ in the first integrator are de-activated, while $V_{dd}/2\text{Gen}$ in the second integrator is activated;
- (iii) the common-mode feedback circuitry of OP1 is refreshed: this process forces the outputs of the op amp to $V_{dd}/2$;
- (iv) in the second stage the integration phase is performed while the switched DAC is de-activated;
- (v) the output of the comparator is not valid.

At the end of phase $K1$, the inputs of the comparator are valid and comparison takes place on the rising edge of $nK1$. Correct operation is guaranteed by providing the necessary setup and hold times with appropriate delays.

During phase $K2$, the following operations take place:

- (i) voltage generators $V_{dd}/2\text{Gen}$ in the first integrator are activated, while $V_{dd}/2\text{Gen}$ in the second integrator is de-activated;

Table 1. Component sizes for Fig. 2.

$C1$ – $C10$	$C11$ – $C14$	$C15, C16$	$R1, R2$	All switches
1 pF	2 pF	8 pF	10 K	$W = 8 \mu\text{m}$, $L = 0.8 \mu\text{m}$

Fig. 2. Switched capacitor implementation of the second order sigma-delta modulator.

- (ii) the switched DAC of the first integrator is de-activated while the switched DAC of the second integrator is activated: resistors $R1$ and $R2$ are used to limit the loading effect of the voltage generator $V_{dd}/2\text{Gen}$ by the input voltage source;
- (iii) the integration phase of the first stage is performed;
- (iv) capacitors $C3$ and $C4$ are pre-charged with the output of the first integrator;
- (v) capacitors $C9$ and $C10$ are pre-charged with the reference voltage;
- (vi) the common-mode feedback circuitry of OP2 is refreshed: this process forces the outputs of the op amp to $V_{dd}/2$;

- (vii) capacitors $C5$ and $C6$ are precharged with a level shift of $V_{dd}/2$;
- (viii) the output of the comparator remains valid.

At the end of $K2$, the output of the comparator is latched using the D-bistables DF1 and DF2: these bistables are used in order to maintain the output valid during phase $K1$, while providing the necessary delay in the feedback loop for the first integrator. These bistables were implemented using standard digital library cells available from the CMOS design kit.

During the start of each integration phase, voltage spikes exceeding the supply voltage can occur at the input nodes of the op amps which can cause charge loss due to leakage current into the bulk in the switching transistors. This effect can severely limit the accuracy

Fig. 3. Switched op amp with common-mode feedback.

Fig. 4. Gain and phase response of the switched op amp.

of the modulator. Capacitors C_{15} and C_{16} attenuate the value of these spikes at the start of K_2 . Since the capacitors are fully discharged during K_2 , they do not affect the final integration result.

2.2. Switched Op Amp

A modified switched op amp [4] is used to implement the integrators. The op amp is based on a differential pair M_0 – M_1 followed by a folded cascode stage M_3 , M_4 , M_7 – M_{10} as shown in Fig. 3. Table 2 shows the

corresponding component sizes. In order to provide sufficient gate over-drive for transistors M_0 – M_1 , the input common mode voltage is set to V_{dd} . Capacitors C_{C1} , C_{C2} and C_F provide common-mode feedback; since the dominant pole in this circuit arises at the output node, C_{C1} and C_{C2} also provide the necessary frequency compensation. Fig. 4 shows the gain and phase response of the op amp which has an open loop gain of 60 dB, a phase margin of 60° and a GBW of 54 MHz. The common mode feedback circuit transistor switches M_{11} , M_{12} are also here outside the signal path.

Table 2. Component sizes for the switched op amp.

	$M0,$ $M1$	$M2$	$M3,$ $M4$	$M5,$ $M6$	$M7,$ $M8$	$M9,$ $M10$	$M11$	$M12$	C_F	$C_{C1},$ C_{C2}
W (μm)	600	5	26	175	782	450	2	2	6 pF	3 pF
L (μm)	1	1	1	1.2	1.2	1	1.2	1		

The op amp operates in two phases: active mode KA (integration phase) and non-active mode KC (common-mode feedback refresh mode with output set to $V_{dd}/2$).

During the non-active mode KC, the following operations take place:

- (i) transistors $M3/M4$ and $M7/M8$ are switched off, thus turning the output stage off;
- (ii) $V_{dd}/2\text{Gen}$ is activated, thus forcing the output to $V_{dd}/2$;
- (iii) capacitors C_{C1} and C_{C2} are pre-charged with a value of $V_{dd}/2$;
- (iv) capacitor C_F is precharged with V_{dd} which is the nominal V_{GS} voltage for the tail current source transistor $M2$.

During the active mode KA, the following operations take place:

- (i) transistors $M3/M4$ and $M7/M8$ are switched back to their normal operation, so that the cascode stage is now active;
- (ii) $V_{dd}/2\text{Gen}$ is switched off;
- (iii) common mode feedback is provided by C_{C1} , C_{C2} and C_F .

Neglecting the parasitic capacitance at the drain terminal of $M12$, the gate voltage of $M2$ during active mode is given by:

$$V_{G2} = \frac{C_C C_F (V_o^+ + V_o^- - 1)}{(2C_C + C_S)(C_{GS2} + C_F)} + 1$$

where

$$C_S = \frac{C_F C_{GS2}}{C_F + C_{GS2}} \quad \text{and} \quad C_C = C_{C1} = C_{C2}$$

Fig. 5. Switched voltage reference.

Fig. 6. Comparator with latch.

This arrangement will keep V_{G2} equal to V_{dd} if the common-mode output voltage is exactly at $V_{dd}/2$. An increase in the output common mode voltage will cause an increase in V_{G2} , thus increasing the current through $M0$ and $M1$, forcing the output common mode voltage to return back to approximately $V_{dd}/2$. This common-mode feedback arrangement allows fast settling of the common mode output voltage to be achieved in a single clock phase. Switching off of the input stage of the op amp has been avoided in this design in order to achieve a reduced turn-on time; the turn-on time is further reduced by the fact that the compensation capacitors are already precharged to $V_{dd}/2$ at the start of the active mode.

2.3. Switched DAC and $V_{dd}/2$ Generator

The reference generator which is based on a resistive network together with the necessary switches is shown in Fig. 5 together with the respective component sizes

Table 3. Component sizes for the switched voltage reference.

	$M1, M2, M5, M6$	$M3, M4, M7, M8$	R	R_{ext}	$C1, C2$
$W (\mu m)$	147	40	10 k Ω	20 k Ω	1 pF
$L (\mu m)$	1.2	1			

in Table 3. Transistors $M1, M2, M3, M4$ are used to switch off the reference generator and set the output nodes to high impedance mode. The digital feedback signals (Q, nQ) control transistors $M5-M8$, which determine whether a positive or negative output reference voltage is generated: when $M6$ and $M7$ are switched on, a positive output voltage is generated, while when $M5$ and $M8$ are switched on, a negative voltage is generated. The value of the differential voltage V_{ref} at the output nodes is given by:

$$V_{ref} = \pm \frac{V_{dd}}{R + R \parallel R_{ext}} (R - R \parallel R_{ext})$$

The resistor R_{ext} is an external resistor, which permits the value of V_{ref} to be adjusted. The inverter

Fig. 7. Simulation transient response of the sigma-delta modulator with zero input, showing the output waveforms for the first and second integrators together with the digital output. The integrator outputs are valid on complementary clock phases.

delay between the gate signals of $M1$ ($M2$) and $M3$ ($M4$) causes a common mode glitch (with a peak value equal to V_{dd} or 0) to occur at the output nodes when the reference generator is switched off. The amplitude of this glitch is reduced by the addition of capacitors $C1$ and $C2$, which keep the voltage across the resistors R approximately constant, until both $M1$ and $M3$ are switched off. The effect of these glitches on the integrated value is further reduced by introducing appropriate delays in the clocking signals such that the integration capacitors are isolated before the DAC is

switched off. The $V_{dd}/2$ generator is based on the same circuit shown in Fig. 5 with $M5$ – $M8$ and R_{ext} omitted.

2.4. Comparator

The comparator uses an n-channel differential pair followed by a regenerative latch circuit as shown in Fig. 6. The corresponding component sizes are shown in Table 4. Transistors $M1$ and $M2$ are the input pair while $M3$ and $M4$ constitute an active load. The common mode input voltage is set to V_{dd} in order to ensure

Fig. 8. Micrograph of the second-order sigma-delta modulator test chip.

Table 4. Component sizes for comparator.

	$M1, M2$	$M3, M4, M5$	$M6, M7$	$M8, M11$	$M9, M10$	$M12, M13$	$M14, M16$	$M15, M17$	R
$W (\mu\text{m})$	100	400	750	200	100	50	50	20	520Ω
$L (\mu\text{m})$	1	1.2	1	1.2	1.2	1	1.2	1	

correct operation of the differential pair. Transistors $M3$ and $M4$ also provide the biasing current of the input pair. The common mode voltage at the drain nodes of $M1$ and $M2$ is set by $M6$ and $M7$. Additional gain is provided by $M12$ and $M13$, which drive the positive feedback latch formed by $M9$ and $M10$. The biasing current through $M12$ and $M13$ is determined by the rel-

ative aspect ratios of $M12, M6$ ($M13, M7$). The latch is reset via transistors $M8$ and $M11$ by driving the COMP signal low: comparison takes place on the rising edge of the COMP signal. The configuration used enables reliable resetting of the latch at low supply voltages since one terminal of the reset transistor is directly connected to V_{dd} . The output of the latch drives an inverter

stage, which generates the required digital signal (0, V_{dd}). Both the output (Q) and its complement (nQ) are generated as required to drive the switched-DAC.

3. Experimental Results

Transient simulations results for the proposed second-order sigma delta modulator are shown in Fig. 7. This figure shows the differential output voltage after the first and second integrator, and the corresponding digital output with zero input condition. The compar-

ator output exhibits the expected digital idle output pattern. A prototype of the proposed second-order sigma delta modulator has been fabricated in a conventional $0.8\ \mu\text{m}$ double-poly, double-metal CMOS process. A microphotograph of the test chip is shown in Fig. 8. The circuit dissipates 1.5 mW from a 1 V supply. The die area of the whole test chip which also includes extra test blocks and probe pads measures $1.8 \times 2\ \text{mm}$.

The modulator was tested at a clock frequency of 500 kHz. The measured noise power spectral density

Fig. 9. Noise power-spectral density of the proposed sigma-delta modulator obtained by Fast Fourier Transform of the output bit-stream.

obtained by Fast Fourier Transform of the sigma-delta modulator output bit stream is shown in Fig. 9. The noise-shaping obtained corresponds to the theory, but a -80 dB white-noise floor appears at low-frequencies. This noise contribution, mainly due to the thermal noise of switches and operational amplifiers and the flicker noise of the input pair, is acceptable when considering the low power supply voltage used (1 V). Fig. 10

shows the signal-to-noise ratio (SNR) of the modulator as a function of the baseband limit. The second-order noise shaping function produces the expected 15 dB/octave slope in the SNR curve. Although at low frequency the thermal noise limits the slope to 3 dB/octave, an oversampling ratio of 64 still ensures a SNR of about 56 dB, corresponding to more than 9 bits of resolution.

Fig. 10. Signal-to-noise ratio (SNR) of the proposed sigma-delta modulator as a function of the baseband limit.

4. Conclusion

A second order sigma-delta modulator operating at 1 V supply has been presented. The main issue in designing low voltage SC circuits is to ensure that the transistor switches can be switched on and off reliably. In this design, this has been achieved by avoiding switches in the signal path and ensuring that one terminal is at V_{dd} or ground potential. This was made possible by using a modified switched op amp integrator, switched half-supply generator and switched DAC. Testing of the fabricated prototype at 1 V shows the expected second order noise-shaping behaviour, and with an oversampling ratio of 64, more than 9 bits of resolution are obtained.

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