The present invention provides an n-bits successive approximation register (SAR) analog-to-digital converting (ADC) circuit, comprising: an n-bits SAR control logic, a p-type capacitor network including a DAC \text{p} array and a sampling capacitor \text{C}_\text{Sp}, an n-type capacitor network including a DAC \text{n} array and a sampling capacitor \text{C}_\text{Sn}; and a comparator for comparing outputs from the p-type capacitor network and the n-type capacitor network, wherein a power supply and ground are directly connected to the p-type capacitor network and the n-type capacitor network without using reference voltages produced by a reference voltage generator. The n-bits SAR control logic comprises \( n \) shift registers, \( n \) bit registers, and a switching logic. The comparator comprises a first pre-amplifier, a second pre-amplifier, and a dynamic latch. Alternatively, the comparator comprises a four-input pre-amplifier and a dynamic latch.

6 Claims, 4 Drawing Sheets
Fig. 3
FIELD OF THE INVENTION

The present invention relates to an n-bits successive approximation register (SAR) analog-to-digital converting (ADC) circuit, and more particularly to a SAR ADC circuit without using the reference voltages produced by a reference voltage generator.

DESCRIPTION OF RELATED ART

Low power is the most relevant design concern for battery-powered mobile applications. Conventionally, a pipeline ADC is commonly used because of its power efficiency. The pipeline architecture does not benefit from the technology scaling because the use of low voltage supplies gives rise to an augmented consumption of power. Recently, a SAR architecture has re-emerged as a valuable alternative to the pipeline solution.

The speed of a SAR ADC circuit is determined by the time required by a digit-to-analog (DAC) circuit to settle within ½-LSB (least significant bit). With large numbers of bits and capacitive arrays, the main cause of power consumption is the reference voltage generator that must provide very low output resistance. The total power dissipation in a SAR ADC is dominated by the reference voltage generator, while the power consumed by the comparator and the switching is a small fraction of the total power.

SUMMARY OF THE INVENTION

The object of the present invention is to provide an n-bits SAR ADC circuit without using the reference voltages produced by a reference voltage generator so as to further improve power efficiency.

According to one aspect of the present invention, there is provided an n-bits SAR ADC circuit, comprising: an n-bits SAR control logic, a p-type capacitor network including a DACp array and sampling capacitance Cs, an n-type capacitor network including a DACn array and a sampling capacitor Cs, and a comparator for comparing outputs from the p-type capacitor network and the n-type capacitor network, wherein a power supply and ground are directly connected to the p-type capacitor network, and the n-type capacitor network without using reference voltages produced by a reference voltage generator.

According to the other aspect of the present invention, the n-bits SAR control logic comprises: n shift registers, n bit registers, and a switching logic.

According to another aspect of the present invention, the comparator comprises: a first pre-amplifier, a second pre-amplifier and a dynamic latch.

FIG. 1 shows a block diagram of the n-bits SAR ADC circuit according to the present invention.

FIG. 2a shows a conceptual sampling scheme and the connecting relationship of the capacitor network and the pre-amplifier shown in FIG. 1.

FIG. 26 shows the successive approximation (SA) conversion scheme, where the output of DAC array converges to the negative sampled signal on Cn at the ref-terminal of the pre-amplifier shown in FIG. 2a.

FIG. 3 shows a block diagram of the comparator shown in FIG. 1.

FIG. 4 shows a block diagram of the SAR control logic shown in FIG. 1.

DETAILED DESCRIPTION OF THE EMBODIMENT

A preferred embodiment of the present invention will be described hereinafter with reference to the accompanying drawings.

First, please refer to FIG. 1. FIG. 1 is a block diagram of the n-bits SAR ADC circuit according to the present invention. As shown in FIG. 1, the n-bits SAR ADC circuit according to the present invention comprises: a SAR control logic (100), a p-type capacitor network (202), an n-type capacitor network (204), and a comparator (300). The p-type capacitor network (202) includes a DACp array (unshown) and a sampling capacitor Cs (unshown). On the other hand, the n-type capacitor network (204) includes a DACn array and a sampling capacitor Cs. The comparator (300) is composed of a first pre-amplifier (302), a second pre-amplifier (304) and a dynamic latch (308). Alternatively, the comparator is composed of a four-input pre-amplifier and a dynamic latch. The SAR control logic (100) provides two series of control signals Sp and Sn to the p-type capacitor network (202) and the n-type capacitor network (204), respectively.

Conventionally, a p-type capacitor network has four inputs including: Vrefp, Vcom, Vrefp, and Vrefp, and a n-type capacitor network has four inputs including: Vrefn, Vcom, Vrefn, and Vrefn. Where Vrefp is the voltage of input analog signal of the p-type capacitor network; Vcom is the voltage of input analog signal of the n-type capacitor network; Vrefp and Vrefn are two reference voltages produced by a reference voltage generator; and Vcom is the voltage of common mode, which is produced by Vrefp and Vrefn, and the value of Vcom is a fraction of Vrefp and Vrefn (Vcom is the middle level of Vrefp and Vrefn). The outputs of p-type capacitor network and n-type capacitor network, including VDACp and VDACn are inputted to a comparator. Subsequently, the output of the comparator is inputted to a SAR control logic. It should be noted that conventional p-type capacitor network and n-type capacitor network do not have the sampling capacitor Cs and Cs, where only two outputs VDACp and VDACn are provided to the comparator.

On the contrary, according to the present invention, as shown in FIG. 1, the p-type capacitor network has four inputs including: Vrefp, Vcom, Vd, and Gn, and the n-type capacitor network has four inputs including: Vrefn, Vcom, Vd, and Gnd. Where Vrefp is the voltage of input analog signal of the p-type capacitor network; Vcom is the voltage of input analog signal of the n-type capacitor network; Vd is the voltage of power supply; Gn is grounded; and Vcom is the voltage of common mode, which is produced by Vd and Gnd, and the value of Vcom is a fraction of Vd and Gnd (Vcom is the middle level of Vd and Gnd). It should be noted that, in the present invention, the capacitor networks use the inputs Vd and Gnd to replace conventional inputs Vrefp and Vrefn which are produced by a reference voltage generator. In addition, according to the present invention, the sampling capacitors Cs and Cs (not shown in FIG. 1) are provided in the p-type capacitor network.
and the n-type capacitor network, respectively. The effect of the sampling capacitors is to provide an opposite input signal to the DAC, which will be described later. In the present invention, the outputs of p-type capacitor network and n-type capacitor network, including \( V_{DACp}, V_{Con}, V_{Cip} \) and \( V_{DACn} \) are input to a comparator. Subsequently, the output of the comparator is input to a SAR control logic. It should be noted that, in the present invention, the p-type capacitor network and the n-type capacitor network totally have four outputs including \( V_{DACp}, V_{Con}, V_{Cip} \) and \( V_{DACn} \) rather than conventional two outputs.

As described above, according to the present invention, the p-type capacitor network includes a DAC array and a sampling capacitor \( C_{Sp} \). Similarly, the n-type capacitor network according to the present invention includes a DAC array and a sampling capacitor \( C_{Sn} \). As shown in Fig. 1, \( V_{DACp} \) denotes the voltage of output of DAC array in the p-type capacitor network; \( V_{DACn} \) denotes the voltage of output of the DAC array in the n-type capacitor network. \( V_{Cip} \) denotes the voltage of output of the sampling capacitor \( C_{Sp} \) in the p-type capacitor network; and \( V_{Con} \) denotes the voltage of output of the sampling capacitor \( C_{Sn} \) in the n-type capacitor network.

On the contrary, the SA algorithm according to the present invention drives the output of DAC array to \(-V_{in}\) instead of zero at the end of the bit-cycling, according to the following formulas (2) and (3):

\[
V_{in} = \sum_{n} S_{n} V_{ref,pro} \quad (2)
\]

\[
V_{in} = \frac{\sum_{n} S_{n} V_{ref,pro}}{C_{DAC,Sum}} \quad (3)
\]

In the above formulas, \( S_{n} (1 \text{ or } 0) \) is the ADC decision for bit \( n \); \( C_{DAC,Sum} \) represent the capacitors connected the reference voltage and the total array capacitance, respectively; \( V_{ref,pro} \) is the reference voltage proposed in the present invention; and \( V_{ref,con} \) is the reference voltage used in a conventional SAR algorithm. As obviously seen from the above Formula (3), the value of \( V_{ref,pro} \) is two times of the value of \( V_{ref,con} \). Therefore, the power supply can be directly used as the reference voltage.

Next, please refer to Fig. 3. Fig. 3 shows a block diagram of the comparator according to the present invention. The comparator pre-amplifier has two differential pairs M1, M2 and M3, M4 connected to the outputs of the differential capacitive DAC and the additional sampling capacitor \( C_{Sp} \). The input differences of M1 to M4 change the currents following through resistive loads \( R_{d} \), which are summed up and appear as the voltage difference to the dynamic latch. The bias current and the load resistance yield a pre-amplifier gain of tens \( dB \). The comparison cycle is divided into a reset phase and a generation phase. During the reset phase (STROBE=0), the pre-amplifier output is shorted to avoid memory effect of the comparison. Moreover, M11-M14 reset the regenerative loop and set the outputs \( V_{op} \) and \( V_{on} \) to \( V_{dd} \). Since the current source transistor M15 is switched off, no current flows from the supply to ground. When the regenerative phase starts (STROBE=1), M15 switches on and the input transistor M5-M6 force currents flowing through back-to-back inverters M7-M8 and M9-M10 to amplify the voltage difference to a full swing.

Next, please refer to Fig. 4. Fig. 4 shows a block diagram of the SAR control logic according to the present invention. As shown in Fig. 4, the SAR control logic according to the present invention comprises a set of shift registers (\( SR_{1} \rightarrow SR_{2n-1} \)), a set of bit registers (\( BR_{1} \rightarrow BR_{2n-1} \)) and a switching logic. The \( CLK \) used to control the shift registers are synchronous with the reset of the comparator. The bit register detects each bit decision from the comparator and locks it for next stage processing.

In summary, the present invention provides a sampling capacitor in the p-type capacitor network and the n-type capacitor network, respectively. In addition, the p-type capacitor network and the n-type capacitor network in the present invention use \( V_{op} \) and \( V_{on} \) to replace conventional reference voltages produced by a reference voltage generator. Accordingly, the present invention can significantly improve the power efficiency of a SAR ADC circuit.

The conventional SA algorithm drives the output of DAC array to zero at the end of the bit-cycling, according to the following formula (1):

\[
V_{in} = \frac{\sum_{n} S_{n} V_{ref,con}}{C_{DAC,Sum}} \to 0
\]
The above description is made with respect to one embodiment of the present invention. However, the present invention is not limited to the above description. People of ordinary skill in the same field may make various modifications to the details of the embodiment without departing from the scope and the spirit of the present invention.

What is claimed is:

1. An n-bits successive approximation register (SAR) analog-to-digital converting (ADC) circuit, comprising:
   a p-type capacitor network including a DAC<sub>p</sub> array and a sampling capacitor C<sub>sp</sub>;
   an n-type capacitor network including a DAC<sub>n</sub> array and a sampling capacitor C<sub>sn</sub>; and
   a comparator for comparing outputs from the p-type capacitor network and the n-type capacitor network, wherein a power supply and ground are directly connected to the p-type capacitor network and the n-type capacitor network without using reference voltages produced by a reference voltage generator.

2. The SAR ADC circuit according to claim 1, wherein the n-bits SAR control logic comprises n shift registers, n-bit registers, and a switching logic.

3. The SAR ADC circuit according to claim 1, wherein the comparator comprises a first pre-amplifier, a second pre-amplifier and a dynamic latch.

4. The SAR ADC circuit according to claim 1, wherein the comparator comprises a four-input pre-amplifier and a dynamic latch.

5. The SAR ADC circuit according to any one of claims 1-4, wherein in the p-type capacitor network and n-type capacitor network, the signal input to the DAC array is opposite to the signal input to the sampling capacitor.

6. The SAR ADC circuit according to any one of claims 1-4, wherein sampling capacitor is selected to provide a voltage -V<sub>m</sub>.