A 256 x 256-Pixel Optical Sensor Architecture with 32 Algorithmic A/D Converters

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Abstract

A 256 x 256-pixel intelligent optical sensor with 32 A/D converters on board is presented. The circuit offers a favourable trade-off between classical architecures based on a single video converter and other architectures involving a very large number of converters. A novel algorithmic A/D converter architecture was designed to achieve the required accuracy at video rate. Fabricated in a 1.2 μm standard CMOS process with an added metal 3 light-shielding layer, the circuit is functional and requires a total area of 50 mm^2.

1. Introduction

Interest for medium-resolution flexible optical sensor arrays for robotics, security, surveillance and industrial control applications is increasing. The main requirements are the capture of good-quality images, ready interfaceability with a digital processor and low power consumption. Classical CCD sensors are limited in their applicability due to their analogue outputs, which require external analogue-to-digital converters operating at video rate and consuming an unnecessary amount of power and synchronisation circuits including dual-port digital memory and control logic. The approaches involving CMOS arrays [1,2] usually rely on one converter per column of photosensors, thus needing n integrating converters for an array of size n^2.

This paper presents a system comprising a square array of n^2 photosensitive elements and an array of n/m converters operating in parallel, where the "interleave factor" m = 8 was chosen to offer a favourable trade-off between the two existing approaches in terms of silicon area, power consumption and speed. A multiplexing scheme is used to sequentially connect the A/D converter to the appropriate pixel column. A novel algorithmic A/D converter was designed as the basic cell of a converter array capable of achieving the required video conversion rate with 8-bit accuracy. The flexibility of the architecture enables its application in arrays with a very fine inter-pixel pitch or at frame rates higher than standard.

2. System architecture

The architecture of the sensor is depicted in the block diagram of Fig. 1. It comprises an array of 256 x 256 photosensors and an array of 32 charge amplifiers and 8-bit A/D converters with associated double-line memory. Photosensor x-y selection, control and I/O logic is provided for direct interface to a microprocessor bus. A study on the required interleave factor showed that the value of one converter every 8 pixel columns was optimal for the target silicon technology. Other interleave factors may be more suitable for different array sizes, operational speeds and/or converter types.

The basic sensing cell is realised with an n^+/p junction [3] operating in the charge storage mode and a selection switch implemented with an n-channel transistor with a size close to the minimum, (W=2 μm, L=1.5 μm) to minimise the leakage current. The size of the basic sensing cell is 20 μm x 20 μm, which leads to a total array size of 5.12 x 5.12 mm^2. Cell selection is achieved by two decoders (row decoder and charge amplifier decoder) which connect one cell at a time to the charge amplifier.

The charge amplifier used to convert the photogenerated charge to a voltage [2] (Fig. 2) is based on a conventional transconductance amplifier. During the reset phase (Φ_{RES}) the integrating capacitor C_F is precharged to the reference voltage V_{RF1}. During the read phase Φ_{RD} it receives the charge stored on the photodiode. The values of V_{RF1} and V_{RF3} chosen optimise the dynamic range of the amplifier. The operation of the charge amplifier is offset-insensitive. During the readout operation, the photodiode is automatically reset to V_{RF3}, as required for the next light integration period.

The signal from the charge amplifier is converted by the ADC (described in detail below). A 2 x 256-byte double-line dynamic memory (Fig. 1) is used to store the digitised data from one pixel row for simultaneous A/D conversion and readout by an external processor. During the A/D conversion of a pixel line, each converted bit is stored on the gate M_3 of the conversion memory cell (Fig. 3) by means of x-y selection strobes on M_1 and M_2. After the pixel line has been entirely converted, the data is transferred to the readout memory cell (M_5) via M_4 and M_6.

3. Algorithmic A/D converter

Fig. 2 shows the circuit diagram of the A/D converter. It is based on a novel algorithmic approach that requires only two matched capacitors ($C_2 = C_{INT} = C$), some switches and a suitable sequence of reference voltages. The A/D converter comprises a charge integrator followed by a comparator. The charge corresponding to the input voltage, Q_{IN}, is initially stored onto C_{INT}. N = 8 conversion steps are then performed, where N is the converter resolution, starting from the most significant bit b_1. The output level of amplifier A_2 is detected by the comparator which, in turn, drives the control logic. This steers the integrator so as to force the residual charge Q_{INT} on C_{INT} to approach the middle of the dynamic range, $CV_R/2$, where $V_R = V_{RF3} - V_{RF1}$.

At any given conversion step after the first one, the control logic sets $\Phi_A = \Phi_1$, $\Phi_B = \Phi_2$ or vice-versa, depending on the result of the previous comparison. Therefore, C_2 performs an inverting or non-inverting injection of charge proportional to the reference voltage V_{DAC}. At each step, V_{DAC}, which is used simultaneously for all 32 A/D converters, is successively divided by two ($V_{DAC}(i) = V_R/2^i$) (Fig. 2). Thus, the total charge injected through C_2 corresponds to a successive approximation of $Q_{IN} - CV_R/2$. The residual charge on C_{INT} at the i-th step is equal to:

$$Q_{INT}(i) = Q_{IN} - C\left[\sum_{2}^{i} 2\left(b_{j-1} - \frac{1}{2}\right)\frac{V_R}{2^j}\right] \qquad (1)$$

where b_j is the j-th bit. At any step, the difference between $V_{OUT} = V_{RF1} + Q_{INT}/C$ and $V_{RF2} = V_{RF1} + V_R/2$ allows the value of the corresponding bit to be determined. The residual charge $Q_{INT}(N)$ approaches $CV_R/2$, and therefore $V_{OUT}(i = N)$ approaches V_{RF2}, as required by the algorithmic search.

The reference voltages V_{RF1} = 1 V, V_{RF2} = 2 V and V_{RF3} = 3 V and the intrinsic level shifting optimise the circuit dynamic range. The choice of the ratio between capacitor values ($C_F = 4C_D$; $C_2 = C_{INT} = C/4$) leads to an overall gain of the structure equal to unity.

The only drawback derives from the slewing requirements in the transition from Φ_1 and Φ_2: the output voltage of A_2 is V_{RF3} during Φ_1 and $V_{RF1} + Q_{INT}(i)/C_{INT}$ during Φ_2. However, the frequency used and the designed op-amp are such as to make the limit acceptable.

The comparator comprises a pair of autozeroed inverters [4] followed by a third inverter and a latch. Autozero, which is needed to compensate for comparator offset, is carried out before any comparison step, thus also helping in recovery from overdrive conditions. The output latch ensures digital output levels and stores the previous information during a whole conversion step, as required for correct operation of the control logic. The operation of the integrator is offset-insensitive. Charge injection due to the opening of switches in the feedback path of the op-amp in the ADC limits the obtainable conversion accuracy. To limit this effect, small-sized transistors and dummy structures were used.

The N reference voltages V_{DAC} are obtained with a conventional R-2R ladder network [5] (Fig. 4). It should be pointed out that the same reference voltage V_{DAC} is needed simultaneously for all the ADC's in the *i*-th step. Therefore, the required voltage is selected at each step by a multiplexer and is fed to all ADC's by means of a single interconnection line, thus achieving considerable area saving.

4. Results

The circuit was fabricated in a 1.2 μm, n-well, single-polysilicon, implanted-capacitor double-metal CMOS technology with the addition of a special metal 3 layer over the passivation acting as a light shield. Total chip area is 50 mm^2 (Fig. 5). The characteristics of the chip are summarised in Table 1.

Functional tests on the entire chip showed a correct operation up to a frame rate of 25 frames/s. Total current consumption is 28 mA at 5 V, with about 20 mA supplied to the analogue circuits and about 8 mA for the digital section including the padring. For the testing of the charge amplifier and A/D converter, a separate chip with one conversion channel was realised. Measurements showed a conversion rate of 60 Ksamples/s and a 0.3% mismatch between C_2 and C_{INT}. A residual clock feedthrough may limit the resolution. Nevertheless, a proper trimmering of the sequence of reference voltage V_{DAC} allowed 8 bits of resolution to be achieved with less than 3 LSB of integral nonlinearity. This performance was obtained with circuitry having a limited area and power overhead as compared to the photosensor array.

5. Acknowledgements

The work was supported by the European Union through ESPRIT Project 7101 "MInOSS". Claudio Mezzena is gratefully acknowledged for his contribution.

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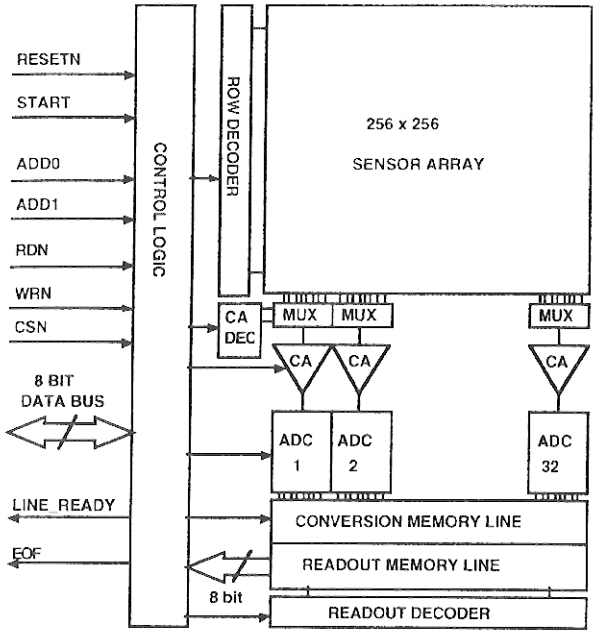

Fig. 1. Block diagram of the sensor chip.

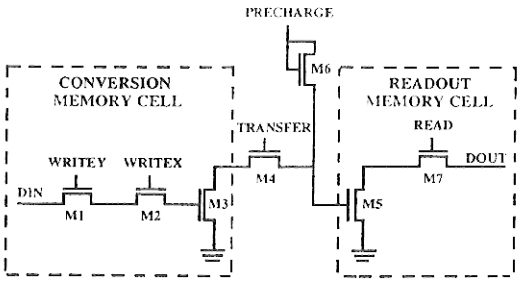

Fig. 3. Double dynamic memory cell.

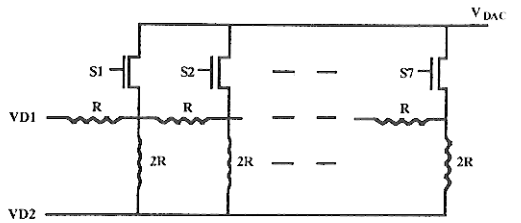

Fig. 4. Reference voltage generator.

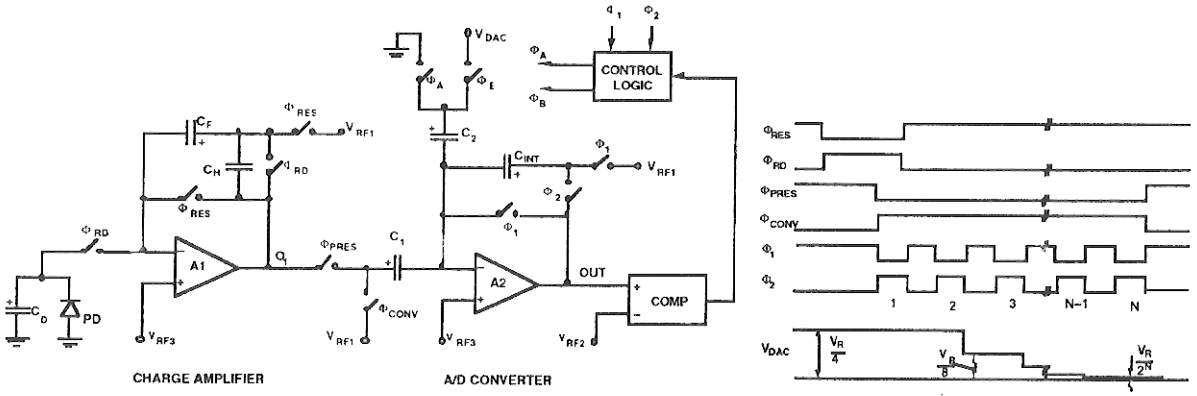

Fig. 2. Charge amplifier and algorithmic converter: schematic (left) and waveforms (right).

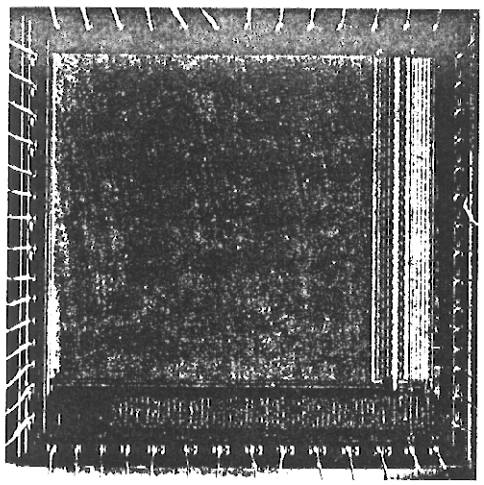

Fig. 5. Microphotograph of the chip.

Array resolution	256 x 256
Pixel pitch	20 μm x 20 μm
Array size	5.12 mm x 5.12 mm
ADC resolution	8 bit
Pixel rate	1.6 MHz
Frame rate	1 - 25 frames/s
Sensor technology	1.2-μm CMOS, 3-metal
Sensor chip size	7.0 x 7.1 = 50 mm^2
Power dissipation	140 mW (5 V, 16 MHz)
Sensitivity	10 lux (with f=1.2)
Spectral range	350 - 900 nm

Table 1. Electro-optical parameters of the intelligent sensor chip.