ANALOG-TO-DIGITAL CONVERTERS FOR OPTICAL SENSOR ARRAYS

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ABSTRACT

The use of CMOS technology allows the monolithic integration of photosensor arrays together with analog-to-digital (A/D) conversion circuits. The structure of the array can be exploited to increase the connectivity between the sensor and the converter, which are in close coupling. Both single-converter per array and multiple-converter per array approaches are therefore possible. This paper presents a comparative study of different A/D conversion architectures incorporated in intelligent optical systems. The presented schemes have been validated by experimental evaluations.

1. INTRODUCTION

Optical sensor systems consist of monolithic arrays of photosensors coupled to selection circuits and signal conditioning: amplification, analog-to-digital (A/D) conversion, interface, analog or digital processing and memory elements. Linear or two-dimensional arrays of photodiodes or phototransistors of size n and n^2, respectively, sense the visible electromagnetic radiation and transform it into a photocurrent. The collected signal is small and, since the band of interest is relatively low, the photosensitive elements operate in the charge storage mode: the photocurrent is integrated on the capacitor associated with the sensor itself for a given time interval [1], [2]. The extraction of the signal from the photosensor area is obtained by x-y selection of each sensor element, realised by decoders or shift registers. Analog processing or memory elements are sometimes associated with each photosensor to achieve functions involving the outputs from neighbouring sensors or successive outputs from the same sensors. The leading trend, however, is to perform the key operation of A/D conversion close to the sensor array to take full advantage of increasingly fast and affordable digital signal processing.

Various A/D conversion architectures operating at different speeds can be used. The choice depends on many trade-offs involving system specifications, chip area, power consumption and required accuracy. This work presents a comparative study of A/D conversion schemes conceived for operation in close coupling with optical sensor systems.

2. SYSTEM FEATURES

An optical sensor system can use a linear or a two-dimensional (2-D) array of optical elements. Linear arrays comprise a relatively limited number of sensors, but operational rates can be high, requiring a correspondingly high data throughput. Stringent requirements must be met in terms of accuracy (in the range from 10 to 14 bits or more, depending on the specific application), absolute non-linearity and temperature stability. In 2-D arrays for machine vision, a much larger number of pixels is required, at generally lower frame frequencies, which usually leads to high data rates. Advanced video systems with 1024×1024 pixels running at 60 Hz require a data output rate of up to 60 Mpixels per second.

3. CONVERTER ARCHITECTURES

The operation speed required of the A/D converter depends on the frame rate and on the number of the pixels in the array. Demanding systems can require a converter accuracy as high as 12 to 14 bits at conversion rates up to 60 Msamples/s. However, for most practical computer vision applications a resolution around 8 bits and a conversion rate of few Msamples/s are sufficient.

Conventional optical sensor systems composed of discrete photosensor arrays and A/D converter (ADC) chips have limited sensor-to-ADC connectivity, which favours single-ADC architectures. This constraint is removed if conversion is performed on chip, because the physical structure of the array can be exploited to greatly increase the number of connections between the sensor array and the converter section. Multiple-converter architectures are thus made possible. Although conversion schemes involving $O(n^2)$ converters have been proposed for 2-D arrays with n^2 pixels, only solutions of $O(n)$ or lower are considered here to be of immediate practical relevance.

Schemes involving n converters were proposed in [3] and [4]. They utilise one converter per column

for 2-D arrays and one per pixel for linear arrays, respectively, directly exploiting the parallelism of the photosensor array. Single-slope integrating converters are employed because of their limited area requirements. The most serious drawback of this architecture, however, is the necessity of matching the pitch of the converters to that of the photosensors, which limits the size of the analog front section and impairs noise performance, gain and offset matching. Technological migration to smaller design rules and pixel pitches in the 5 - 10 μm range will pose a serious constraint on the analog sections as a large number of sense amplifiers are needed to interface the ADC(s) with the photosensors.

To solve this difficulty, two different data converter architectures are proposed here: 1) a single converter architecture and 2) *n/m* converter architecture with an "interleave factor" of *m*. These allow speed, area and noise performance to be traded off in an optimal fashion depending on the application and offer a simplified migration path as design rules and pixel pitches are reduced.

Different converter types were used: a three-step flash, a charge redistribution and a serial (cyclic) ADC. The three-step flash and serial ADC's are optimised for the single-converter configuration, while the charge redistribution scheme is suited for parallel operation with *n/m* converters. The sensor arrays and ADC's (including the required charge amplifiers) were incorporated in intelligent optical systems to validate and compare the different approaches. The same conventional single-polysilicon implanted-capacitor 1.2-μm n-well CMOS process was used for all the circuits, which permits a direct performance comparison.

3.1 Three-step flash converter

A single-converter architecture resembling that of discrete systems was designed to achieve optimal spatial uniformity in conjunction with an on-chip 256×256-pixel array derived from [5] at a frame rate of 30 s^{-1} (pixel pitch: 20 μm × 20 μm). The ADC (output word: 9 bits) is based on a three-step flash principle (Fig. 1) which limits the number of components, and hence area and power consumption. It operates in four phases. During the first phase, the input signal is sampled on internal capacitors. The sampled signal is then held until the next sampling phase. During the second, the third and the fourth phases, the sampled analog voltage undergoes a coarse, an intermediate and a fine A/D conversion, respectively, which determine the *N1* most significant, the *N2* intermediate and the *N3* least significant bits. The bits obtained are finally synchronised to deliver an (*N1* + *N2* + *N3*)-bit digital word. In the present case, *N1* = *N2* = *N3* = 3. Therefore, each sample is converted into a 9-bit word. As the same conversion cells are used for each conversion step, this approach provides silicon area saving with respect to a two-step 4-bit-flash conversion (2 × 4 = 8 bits), while allowing the use of a reasonable conversion speed.

Coarse, intermediate and fine conversions are performed with a flash approach. The reference voltages required for the A/D conversion steps are generated by resistive strings, each consisting of 8 identical polysilicon resistors. To generate the intermediate and fine reference voltages, the corresponding string is connected in parallel to the bottom resistor of the preceding (more significant) one. The loading effect due to this parallel connection is cancelled by injecting an adequate amount of current into the parallel-connected intermediate/fine string [6]. The same resistive strings are also used to generate the reference voltages for the digital-to-analog (D/A) conversions.

A bank of 7 identical conversion cells is used to perform both the subtraction which provides the residues and the successive comparisons for all conversion steps. Each conversion cell (Fig. 2) comprises a comparator and three capacitors. After sampling the input analog signal on input capacitors C_1 of all conversion cells, the comparator bank performs three successive comparison steps (coarse, intermediate and fine). The required reference voltages are successively applied to the capacitors to obtain the residues by using the capacitive redistribution approach.

The overall active area of the ADC and charge amplifier is 4.5 mm^2. Current consumption is 6 mA. Operation of the ADC converter cell and of the digital camera was tested at 8-bit resolution and a conversion rate of 2 Msamples/s corresponding to a frame rate of 30 s^{-1}. Other features are listed in Table I.

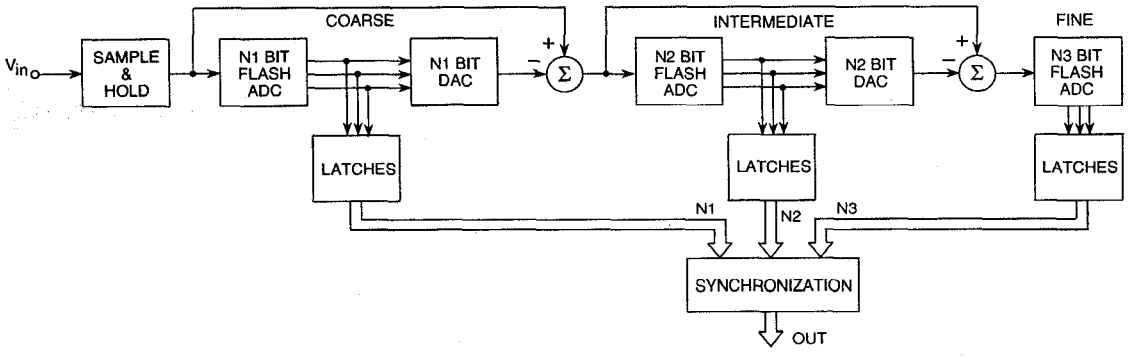

Fig. 1. Architecture of the three-step flash A/D converter.

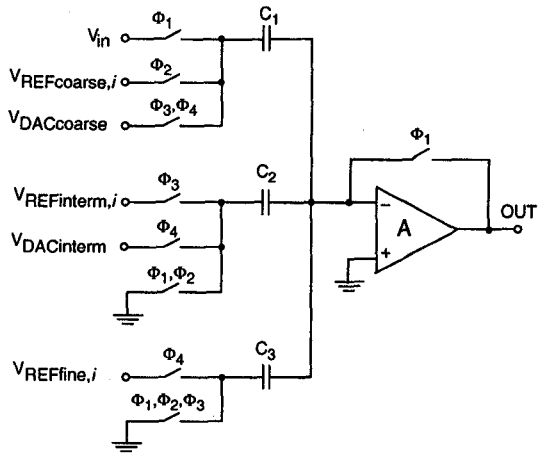

Fig. 2. Elementary cell of the 3-step flash ADC (i = 1 to 7). Φ_1 to Φ_4 are nonoverlapping phases.

3.2 Charge redistribution converter

A charge redistribution converter was developed for use in conjunction with an on-chip 256×256-pixel photosensor array [7] (the pixel pitch was again 20 μm × 20 μm). A parallel architecture comprising n/m-converters was used to provide the required speed while allowing a favourable form factor to be used in the layout. An interleave factor of m = 8 was used in the design (one converter is multiplexed to 8 pixel columns). The ADC (Fig. 3) is based on an algorithmic approach that requires only two matched capacitors, a number of switches and a suitable sequence of reference voltages. The ADC comprises a charge integrator followed by a comparator. The charge corresponding to the input voltage is stored onto C_{INT} and N = 8 conversion steps are then performed, where N is the converter resolution, starting from the most significant bit. The output level of the op-amp is detected by the comparator which, in turn, drives the control logic. This steers the integrator so as to force the residual charge on C_{INT} to approach the middle of the dynamic range.

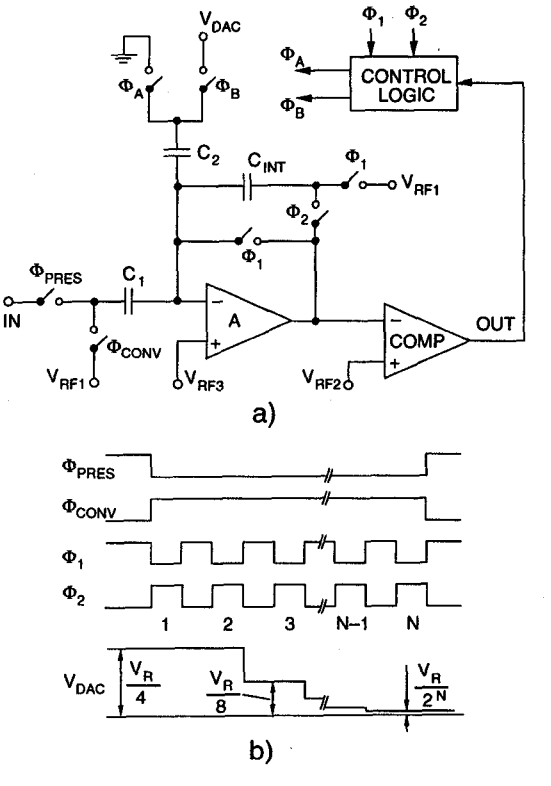

Fig. 3. Charge redistribution converter: (a) schematic diagram; (b) timing diagram.

The N reference voltages V_{DAC} are obtained with a conventional R-2R ladder network serving the entire array of converters. The sizing of the capacitors is chosen to provide unity gain. The scheme used and the operational frequency employed mitigate the slewing requirements on the op-amp.

The comparator consists of two autozeroed inverters followed by a third inverter and a latch. Autozero, which is needed to compensate for comparator offset, is carried out before any comparison step, thus also helping in recovery from overdrive conditions. The output latch ensures digital output levels and stores the previous information during a whole conversion step, as required for correct operation of the control logic. Charge injection due to the opening of switches in the feedback path of the op-amp in the ADC limits the obtainable conversion accuracy. To limit this effect, small-sized transistors and dummy structures were used.

The converter area is 0.125 mm^2 (4 mm^2 for the array) including the charge amplifiers and a double line memory latch for the output data. The width of the converter cell is 160 μm, pitch-matched to eight pixel columns. Total current consumption is 0.6 mA (20 mA for the array) at 5 V. Functional tests on complete digital camera chip showed a correct operation up to a frame rate of 25 s^{-1} corresponding to a conversion rate of 51.2 Ksamples/s per single ADC. A residual clock feedthrough may limit the resolution. A proper trimming of the sequence of reference voltage V_{DAC} allowed 8 bits of resolution to be achieved with less than 3 LSB's of integral nonlinearity.

3.3 Serial converter

A serial converter based on [8] and made available to us as a library cell was employed in conjunction with a 512 linear photodiode array for spectrophotometry (pitch 10 μm × 1 mm) [9]. The instrumentation application at hand required a resolution of 10 bits, a conversion rate of 20 Ksamples/s and good absolute linearity. This was achieved by the use of an algorithmic converter which exploits the redundant signed digit (RSD) principle (Fig. 4) to correct both the error introduced on the gain factor of 2 and offset errors. The gain error resulting from switched-capacitor mismatches was corrected by a strategy implementing an exact multiplication by four after two cycles. A fully-differential topology was used to obtain the best converter performance. The ADC comprises 2

OTA's, capacitors, 2 comparators and control logic for a total area of 2.6×1.0 mm^2. Reported non-linearities are on the order of 0.5 LSB and offset around 0.3 mV at the operating frequency.

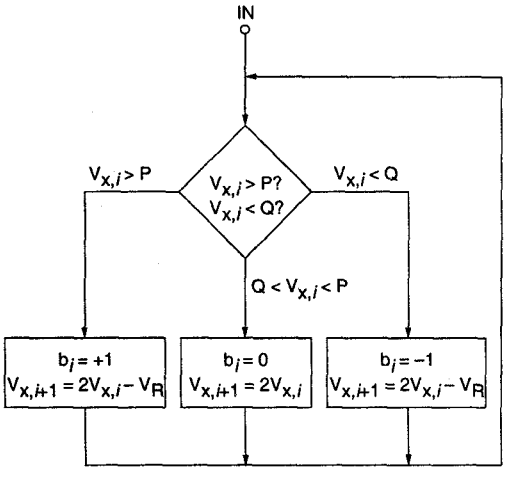

Fig. 4. Basic algorithm of the RSD cyclic converter [8] ($-V_R/2 < Q < 0 < P < V_R/2$). The binary code is obtained by subtracting the negative values ($b_i = -1$) from the output signal.

4. COMPARISON

The results of the preliminary measurements which were carried out on the test intelligent arrays have validated the architectures proposed. Table I shows a comparison of the main characteristics. The performance of the integrating ADC refers to [3]. Area requirements are similar and rather limited in all cases: for the 2D arrays, the area of the ADC was around 16 % of the pixel array area; for the linear sensor, this ratio was 50%. In the charge redistribution ADC, as 50% of the area is taken up by logic components, it can be significantly reduced by the use of sub-micron technologies. The required resolution and operation speed are obtained by all the architectures investigated. A higher frame rate is obviously achieved by the highly-parallel architecture using an integrating converter per each pixel column. However, this is obtained at the expense of a higher power consumption. The use of a single converter and charge amplifier for the whole array minimizes power dissipation and fixed pattern noise.

TABLE I

PERFORMANCE COMPARISON

	3-step flash	charge redist.	serial [8]	integ. [3]
ADC array size	-	32	-	256
Area (mm^2) *				
single ADC	4.5	0.125	2.7	0.01
array	-	4.0	-	2.5
Conv. rate (s^{-1})				
single ADC	2 M	51 K	25 K	78 K
array	-	1.6 M	-	20 M
Resolution (bits)	8	8	11	8
Current cons. * (mA)	6	20	4.8	36^
Fixed pattern noise (dB)	0	–38	0	n.a.
Noise (LSB)	1	2	0.5	2
INL (LSB)	2	3	0.5	2

* ADC(s) + charge amplifier(s)
^ ADC + photosensor array chip

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