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A FULLY INTEGRATED CMOS MAGNETIC CURRENT MONITOR

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ABSTRACT

In this paper we present a fully-integrated magnetic current monitor, which allows accurate and non-invasive current measurements in industrial apparates. The magnetic field generated by the current to be measured is sensed by a Hall device, amplified, converted into the digital domain with 9 bits of resolution and delivered to an on-board I^2S serial interface. The voltage amplifier provides digitally programmable gain and offset. On-chip zener-zapping circuits are used as PROM to store the gain and offset calibration words. Two different operating ranges (20 A and 200 A full scale) are available with independent calibration coefficients. A prototype of the complete microsystem has been integrated in a conventional 0.8 µm CMOS process. Experimental results are presented.

1. INTRODUCTION

Modern electrical apparates, such as soldering machines, car engines (batteries), industrial plants and several others, require accurate, reliable and non-invasive monitoring of currents. It is well known that a current flowing in a conductor produces a magnetic field proportional to the current itself. The value of this magnetic field can be used to measure the current without perturbing or interrupting the conductor. Current monitors based on magnetic field measurements are, therefore, becoming very popular.

The level of magnetic field involved in the measurement of large currents (tens of A) can be easily detected by silicon magnetic sensors fabricated in conventional CMOS technologies, such as Hall devices [1]. It is, therefore, possible to realize low cost single chips containing both the magnetic sensor and the interface circuits required to perform an accurate current measurement [2].

In this paper we present a fully integrated CMOS current monitor, which allows non-invasive (contactless) and inexpensive current measurements. The proposed device supports two different current ranges (20 A and 200 A full scale) and provides a 9-bit digital output through an on-chip I^2S serial interface. Moreover, the system allows gain and offset calibration with an on-chip PROM.

2. CURRENT MONITOR ARCHITECTURE

The block diagram of the proposed current monitor is shown in Fig. 1, while the most important specifications are summarized in Tab. 1. A magnetic sensor detects the magnetic field generated by the current to be measured, enhanced by a suitable ferromagnetic field concentrator, and produces a voltage output signal. This voltage is amplified, converted into the digital domain by a 9 bit successive approximation ADC and delivered to an on-chip I^2S serial interface [3]. In order to achieve an overall accuracy below 1%, we program digitally the gain and the offset of the amplifier. Zener-zapping circuits are used as PROM to store the gain (8 bit) and offset (7 bit plus sign) control words. The two different operating ranges (20 A and 200 A full scale) have independent offset and gain calibration coefficients.

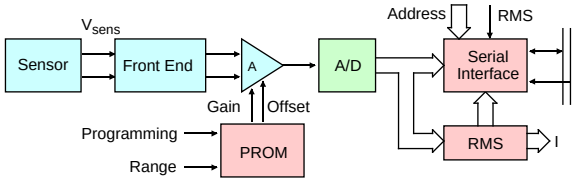

Figure 1. Block diagram of the current monitor

The magnetic sensor used is a spinning current Hall device [4], which produces an output voltage proportional to the magnetic field component perpendicular to the chip plane with very low offset. The sensitivity of this particular device, operated with 1 mA of bias current, is equal to

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Parameter	*Value*
Current Ranges	20A Full Scale 200 A Full Scale
Resolution	9 bits
Accuracy	1%
Output signals	Digital Parallel Digital Serial (I^2S)
Power Supply Voltage	5 V
Technology	CMOS
Clock Frequency	256 kHz

Table 1. Specifications of the current monitor

200 µV / mT. With the field concentrators used, the magnetic field component perpendicular to the chip is equal to 50 mT full scale for the 20 A current range and 500 mT full scale for the 200 A current range, thus leading to sensor output voltages of 10 mV and 100 mV full scale, respectively.

3. INTERFACE CIRCUIT DESCRIPTION

The relatively small voltage signal obtained at the output of the sensor needs to be amplified and converted into the digital domain. The nominal gain required to exploit the whole input range of the A/D converter (±1.25 V full scale) is 125 for the 20 A current range or 12.5 for the 200 A current range. However, since the performance of the sensor and the amplifier (sensitivity, offset and gain) are subject to significant process dependent variations, the gain and the offset of the amplifier should be programmable in order to avoid degradation of the overall system accuracy.

Fig. 2 and Tab. 2 show the schematic and the component values of the programmable gain amplifier, respectively. The circuit consists of an instrumentation amplifier with a fixed gain of 10, followed by a switched capacitor amplifier [5] with binary-weighted capacitor banks to allow offset and gain calibration.

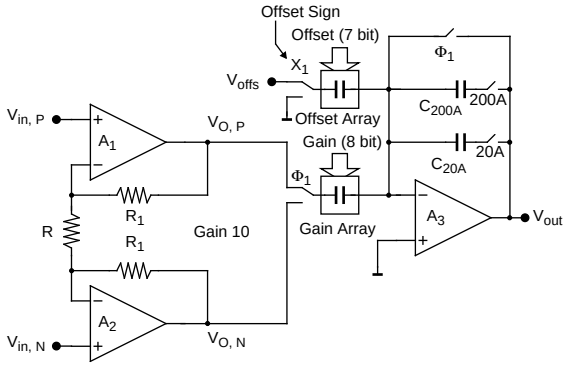

Figure 2. Schematic of the amplifier with programmable gain and offset used in the current monitor

Component	*Value*
Gain Array	28 pF ÷ 91.75 pF
Fixed Capacitance	28 pF
Programmable Capacitance	63.75 pF
LSB	250 fF
Number of Bits	8
Offset Array	0 pF ÷ 31.75 pF
Fixed Capacitance	0 pF
Programmable Capacitance	31.75 pF
LSB	250 fF
Number of Bits	7
C_{200A} (200 A Current range)	47.5 pF
C_{20A} (20 A Current range)	4.75 pF
R (Instrumentation Amplifier)	12 kΩ
R_1 (Instrumentation Amplifier)	54 kΩ
Clock Frequency	256 kHz

Table 2. Component values used in the switched-capacitor programmable-gain amplifier

The programmable gain amplifier operates with two non-overlapping clock phases (Φ_1 and Φ_2). During clock phase Φ_1, the feedback capacitor corresponding to the selected current range (C_{200A} or C_{20A}) is reset, while the operational amplifier is in unity-gain configuration. At the same time, the positive output signal of the instrumentation amplifier ($V_{O,P}$) is sampled onto the *Gain Array* while, depending on *Offset Sign* (through clock phases X_1 and X_2), the *Offset Array* is reset (negative offset, $X_1 = \Phi_2$ and $X_2 = \Phi_1$) or precharged to V_{offs} (positive offset, $X_1 = \Phi_1$ and $X_2 = \Phi_2$).

By contrast, during clock phase Φ_2, we connect the *Gain Array* to the negative output of the instrumentation amplifier ($V_{O,N}$), while the *Offset Array* is connected to V_{ofs} or reset, depending on *Offset Sign*. In view of the charge transfer form the *Gain Array* and the *Offset Array* to the selected feedback capacitor ($C_F = C_{200A}$ or $C_F = C_{20A}$), the output voltage V_{out} becomes

$$V_{out} = (V_{O,P} - V_{O,N})\frac{C_G}{C_F} \pm V_{ofs}\frac{C_O}{C_F}, \qquad (1)$$

where C_G denotes the *Gain Array* and C_O the *Offset Array*. Obviously, the gain and the offset of the amplifier vary when we change the *Gain* and *Offset* control words and hence the values of C_G and C_O.

The operational amplifiers A_1 and A_2 have a folded-cascode structure followed by a low-impedance output buffer, while A_3 is a two-stages operational amplifier with Miller compensation. Complementary CMOS switches and delayed clock phases are used to reduce the clock-feedthrough and charge injection effects.

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The A/D converter, based on the successive approximation algorithm [6], consists of a 9-bit resistive-string D/A converter, a comparator with sample-and-hold and a digital successive approximation register (SAR).

The 9-bit output word of the A/D converter is directly connected to the output pads (parallel output) and, at the same time, delivered to the on-chip bus interface, implementing the two-wires (clock and data) serial protocol I^2S. This protocol allows us to connect up to eight current monitor chips (identified by a 3-bit hardware address) with a single bus master (typically a microprocessor). When the bus master needs to read-out the measurement of a particular current monitor chip, it transmits the corresponding address on the data line (synchronous with the bus clock). All of the current monitor chips receive the address and the interrogated device transmits back the required measurement. The data on the bus are transmitted using the Winchester code in order to allow error detection and arbitration of conflicts. The implemented I^2S serial interface operates with a bus clock frequency up to 100 kHz.

The clock signal used in the whole system is generated by an on-chip RC oscillator.

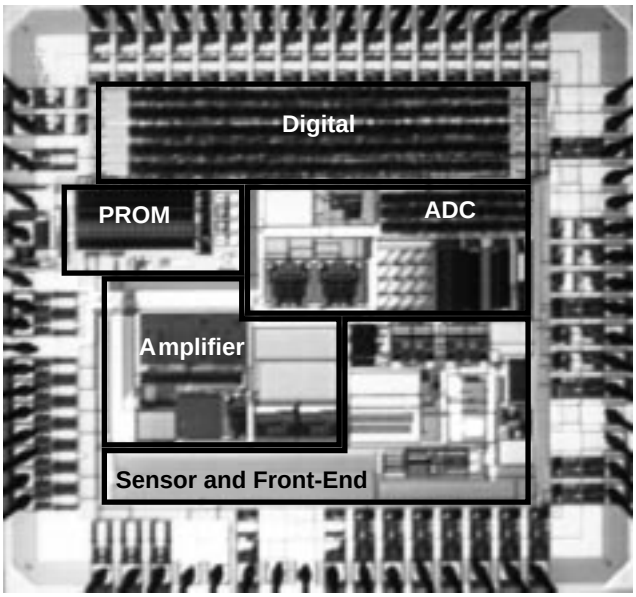

Figure 3. Micrograph of the current monitor chip

4. EXPERIMENTAL RESULTS

A prototype of the proposed current monitor has been integrated in a standard 0.8 µm CMOS technology. The chip micrograph of the chip is shown in Fig. 3. The die area, including pads is 3.2 mm × 3.1 mm.

The measured transfer characteristics of the amplifier chain (instrumentation amplifier and programmable gain amplifier) for the high and the low current range (200 A and 20 A) are shown in Fig. 4 and Fig. 5, respectively. These transfer characteristics demonstrate the gain programmability range of the amplifier (8 bits).

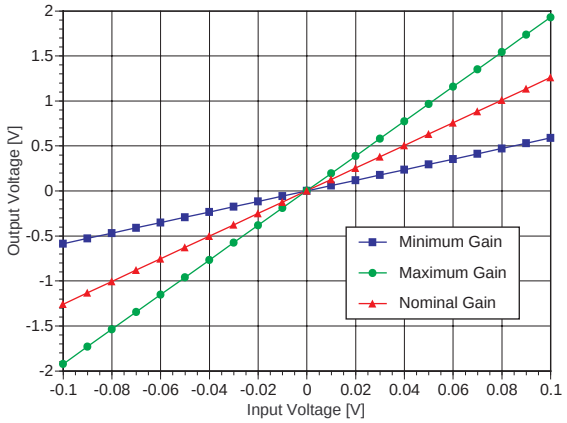

Figure 4. Transfer characteristic of the amplifier chain for the high-current range with *Gain* set to minimum, maximum and nominal

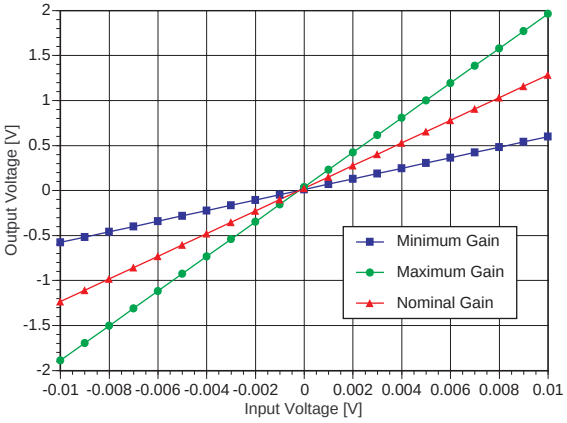

Figure 5. Transfer characteristic of the amplifier chain for the low-current range with *Gain* set to minimum, maximum and nominal

The output signal of the amplifier chain as a function of the offset programming word is shown in Fig. 6. The obtained offset compensation range ensures proper offset cancellation under any conditions.

The measured integral (*INL*) and differential (*DNL*) nonlinearities of the current monitor interface circuit are reported in Fig. 7 and Fig. 8, respectively. We achieved a *DNL* and an *INL* of ±0.6 LSB, corresponding to almost 9 bits of resolution.

Finally, Fig. 9 shows the waveforms (clock and Winchester coded data) of the I^2S serial interface. The characterization of the chip under real operating conditions is in progress.

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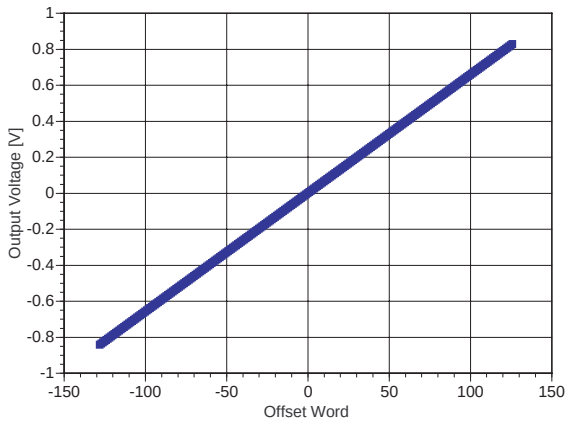

Figure 6. Transfer characteristic of the offset compensation circuit

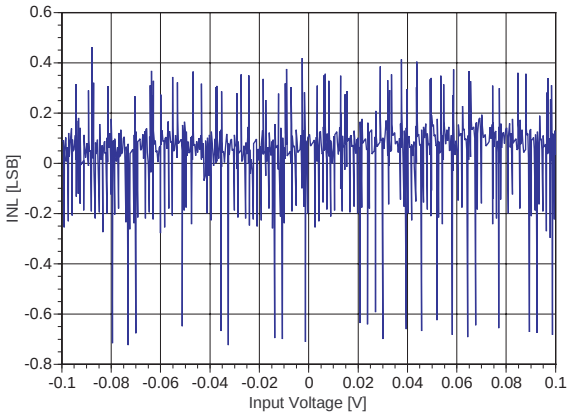

Figure 7. Integral nonlinearity of the current monitor interface circuit

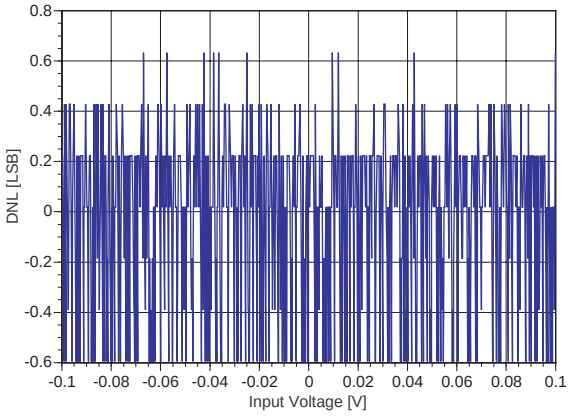

Figure 8. Differential nonlinearity of the current monitor interface circuit

5. CONCLUSIONS

In this paper we presented an integrated magnetic microsystem for non-invasive current measurements. The magnetic field generated by the current to be measured is sensed by a Hall device, amplified, converted into the digital domain and delivered to an on-board I^2S serial interface. The system supports two different operating ranges (20 A and 200 A full scale) and provides digitally programmable gain and offset with an on-chip PROM. The microsystem, integrated in a conventional 0.8 µm CMOS process, achieves 9 bits of resolution and ±0.6 LSB of linearity.

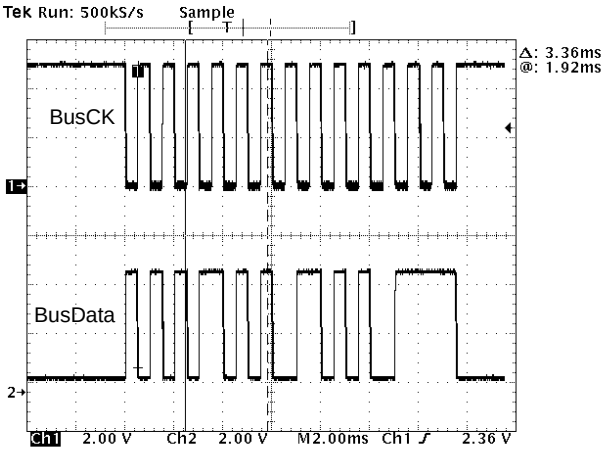

Figure 9. Clock and Winchester coded data waveforms of the I^2S serial interface

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