Design of a 70-MHz IF 10-MHz Bandwidth Bandpass ΣΔ Modulator for WCDMA Applications

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Abstract—In this paper we present a MASH bandpass ΣΔ modulator for WCDMA applications. The signal bandwidth of the proposed modulator is 10 MHz, centered around an intermediate frequency (IF) of 70 MHz. Each ΣΔ modulator of the MASH structure is based on a two-path architecture, which allow us to obtain the desired in-band noise shaping zeros and reduce the power consumption. The ΣΔ modulator is implemented using a 0.18-µm CMOS technology and a sampling frequency of 180 MHz. The simulations at transistor level show a resolution of about 13 bits, with a bandwidth of 10 MHz, and a power consumption of about 90 mW, with a supply voltage of 1.8 V, resulting in a figure of merit (FoM) as low as about 0.15 pJ/conversion-level.

I. INTRODUCTION

In modern communication systems, the direct conversion into the digital domain of the signal at the intermediate frequency (IF), typically in the range 40÷100 MHz, is becoming quite popular. These communication standards foresee wide signal bands (1 ÷ 10 MHz), while requiring medium-high resolution (10 ÷ 14 bits). Since high-resolution Nyquist-rate A/D converters with sampling-rate embracing the IF interval consume significant power, their use is only affordable in base stations. In portable applications, bandpass ΣΔ modulators [1]–[3] are preferable because they consume low power either in continuous-time and sampled-data implementations.

In this paper the design of a bandpass ΣΔ modulator for WCDMA (Wideband Code Division Multiple Access) applications is presented. The considered IF is 70 MHz, the signal bandwidth is 10 MHz, and the signal-to-noise ratio (SNR) target is more than 80 dB. The proposed bandpass ΣΔ modulator is based on a MASH (multi-stage noise shaping) architecture, which realizes a noise transfer function (NTF) with four couple of complex conjugate zeros around the unit circle. The MASH structure consists of two second-order bandpass ΣΔ modulators, each implemented with a two-path architecture with cross-coupled integrators. The two-path architecture allows us to reduce the power consumption and easily implement the desired NTF zeros. The ΣΔ modulator works with a sampling frequency of 180 MHz, so that each path runs at 90 MHz.

The proposed ΣΔ modulator is implemented at the transistor level using a 0.18-µm CMOS technology and a voltage supply of 1.8 V. The adopted architecture is described in Section II, while Section III presents the modulator and resonator design using the two-path approach. Finally, Section IV and Section V present the behavioral and transistor-level simulation results, respectively.

II. ΣΔ MODULATOR ARCHITECTURE

The proposed ΣΔ modulator features a noise transfer function (NTF), given by

\[ NTF = \prod_{i=1}^{4} \left(1 + a_i z^{-1} + z^{-2}\right), \tag{1} \]

where \(a_i (i = 1, 2, 3, 4)\) are real coefficients in the range \([-2, 2]\) to have complex zeros. Fig. 1 shows the position of the zeros around the unit circle, with the chosen values of coefficients \(a_1 = 12/8, a_2 = 13/8, a_3 = 14/8, a_4 = 15/8\). With these values, the zeros are very close to the 0 axis, reducing the complexity of the first Nyquist band.

The proposed ΣΔ modulator architecture, illustrated in Fig. 2, is based on a two-stage MASH structure: the first stage \((\Delta\Sigma_1)\) realizes the external zeros, corresponding to \(a_1 = 12/8\) and \(a_2 = 15/8\), while the second stage \((\Delta\Sigma_2)\) implements the zeros corresponding to \(a_2 = 13/8\) and \(a_3 = 14/8\). This leads…
to a first modulator \( NTF \) given by

\[
NTF_1 = \left( 1 + a_1z^{-1} + z^{-2} \right) \left( 1 + a_2z^{-1} + z^{-2} \right),
\]

while the \( NTF \) of the second modulator turns out to be

\[
NTF_2 = \left( 1 + a_2z^{-1} + z^{-2} \right) \left( 1 + a_3z^{-1} + z^{-2} \right).
\]

Being a MASH architecture, the second modulator receives as input the quantization error \( \epsilon_i \) of the first modulator, and the two digital outputs, \( Y_1 \) and \( Y_2 \), are processed by a digital filter, to cancel the quantization error of the first modulator and realize the overall \( NTF \) given by (1).

By inspection of the circuit, the outputs of the first and second modulator are given by

\[
\begin{align*}
Y_1 &= \text{In} \cdot \text{STF}_1 + \epsilon_1 \cdot \text{NTF}_1, \\
Y_2 &= \epsilon_1 \cdot \text{STF}_2 + \epsilon_2 \cdot \text{NTF}_2,
\end{align*}
\]

where \( \text{STF}_1 = \text{STF}_2 = z^{-2} \) are the signal transfer functions of each modulator. The digital filter implements the function

\[
\text{Out} = Y_1 \cdot z^{-2} - Y_2 \cdot \text{NTF}_1,
\]

thus canceling the quantization error of the first modulator of the form \( \text{STF}_1 \) and leading to the desired output, given by

\[
\text{Out} = \text{In} \cdot z^{-4} + \epsilon_2 \cdot \prod_{i=1}^{4} \left( 1 + a_i z^{-1} + z^{-2} \right).
\]

Both bandpass \( \Sigma \Delta \) modulators used in the MASH structure are based on the same architecture, whose block diagram is shown in Fig. 3. This modulator realizes a \( \text{NTF} \) with two complex conjugate zeros. The values of the coefficients for the two modulators are different: for modulator \( \Sigma \Delta_1 \) we used \( a_j = 12/8 = a_1 \) and \( a_i = 15/8 = a_4 \), while for modulator \( \Sigma \Delta_2 \) we used \( a_j = 13/8 = a_2 \) and \( a_i = 14/8 = a_3 \).

To implement the desired \( \text{NTF} \), each \( \Sigma \Delta \) modulator requires two resonators with transfer function

\[
H_{\epsilon,j}(z) = \frac{z^{-1}}{1 + a_j z^{-1} + z^{-2}}.
\]

As a result, the \( \text{STF} \) is

\[
\text{STF} = \frac{z^{-2}}{D_1 D_j - P_1 z^{-2} - P_2 z^{-1} D_j},
\]

where \( D_{\epsilon,j} = 1 + a_j z^{-1} + z^{-2} \). Since the degree of the denominator of this \( \text{STF} \) is four, it is necessary to adjust the value of four parameters to make it equal to 1. Therefore, the blocks \( P_1(z) \) and \( P_2(z) \) must of the form \( P_1(z) = b_1 + c_1 z^{-1} \) and \( P_2(z) = b_2 + c_2 z^{-1} \), respectively. The values of coefficients \( b_1 \), \( b_2 \), \( c_1 \), and \( c_2 \) that lead to \( \text{STF} = z^{-2} \) are obtained by solving the system of equations

\[
\begin{align*}
1 - c_2 &= 0 \\
2 + a_1 a_i - b_1 - b_2 a_j - c_2 &= 0 \\
a_j - b_1 - c_1 - b_2 - c_2 a_j &= 0 \\
a_i + a_j - b_2 &= 0.
\end{align*}
\]

III. \( \Sigma \Delta \) MODULATOR DESIGN

A power-effective method to implement the \( \Sigma \Delta \) modulator of Fig. 3 is to use a two-path architecture, with twice the number of operational amplifiers (opamps), operated at half of the clock frequency \( (F_s/2 = 90 \text{ MHz}) \). The power consumption of each opamp is almost divided by four and the overall power consumption is then halved. Fig. 4 shows the adopted solution to implement the bandpass \( \Sigma \Delta \) modulator of Fig. 3, using the two-path design approach.

The even and odd input samples are applied to the input of the top and bottom path, respectively, at the sampling rate \( (F_s) \). The feedback coefficients used to make the \( \text{STF} \) denominator equal to one are realized with direct \( (c_1 \) and \( c_2 \)) or cross-coupled paths \( (b_1 \) and \( b_2 \)). At the \( \Sigma \Delta \) modulator output the digital data are taken alternatively from both paths at sampling frequency \( F_s \). The modulator is realized using four switched-capacitor (SC) integrators and two 5-bit flash ADCs. Since the solutions of (9) are integer multiples of the fraction 1/8, with the considered values of coefficients \( a_i \) \((i = 1, 2, 3, 4)\), it is relatively easy to implement the feedback coefficients by capacitive ratios in the SC circuits.
By adding the values of \( F \) in Fig. 6, implementation of the transfer function easily realizes a square wave modulation at \( F_s/4 \) (\( z \rightarrow -z \) transformation) [4] at the input and at the output of a conventional integrator with transfer function

\[
H(z) = \frac{z^{-1/2}}{1 - z^{-1}},
\]

as conceptually explained in Fig. 6, thus implementing the transfer function

\[
\hat{H}(z) = \frac{z^{-1}}{1 + z^{-2}}.
\]

Moreover, suitable cross-coupled feedback paths in the integrators allow us to obtain the \( a_{ij}z^{-1} \) terms in the resonator transfer function.

Considering the block diagram of Fig. 5, the output signals \( P_1 \) and \( P_2 \) are given by

\[
\begin{align*}
P_1 &= (I_{n1} - a_j P_2) \frac{z^{-1}}{1 + z^{-2}}, \\
P_2 &= (I_{n1} - a_j P_1) \frac{z^{-1}}{1 + z^{-2}}.
\end{align*}
\]

By adding the values of \( P_1 \) and \( P_2 \) given by (12), we obtain

\[
P_1 + P_2 = \frac{z^{-1}}{1 + a_{ij}z^{-1} + z^{-2}} (I_{n1} + I_{n2}),
\]

leading to the desired expression of \( H_{i,j} \), given by (7).

### IV. Behavioral Simulation Results

The proposed MASH bandpass \( \Sigma \Delta \) modulator architecture was verified at the behavioral level using Matlab-Simulink\textsuperscript{TM}. The simulations are carried-out with oversampling ratio (OSR) equal to 9 and input frequency around 70 MHz (\( F_{\text{in}} = F_s \cdot N_{\text{per}}/N \), where \( F_s = 180 \) MHz is the sampling frequency, \( N_{\text{per}} = 839 \)) is the prime number of periods of the input signal considered, and \( N = 2^{11} \) is the number of points used in the FFT). Fig. 7 shows the output spectrum under ideal conditions. In the spectrum it is possible to clearly note the four couples of complex zeros in the signal band. The obtained SNR is higher than 115 dB.

The errors in the actual values of the coefficients, caused by real integrators and capacitive mismatches, affect the STF and the NTF of both modulators of the MASH structure. In particular, in order to guarantee the stability of the modulator, we have to make sure that, in spite of any errors, the poles of the NTF do not fall outside the unity circle. Moreover, since the digital filter has to remove the first modulator quantization noise (shaped by its NTF), the implementation of the first modulator NTF has to be carefully considered. The MASH structure is, hence, analyzed using real integrators using a specific toolbox [5]. The used integrators parameters are: DC gain around 1000, slew-rate of 500 V/\( \mu \)s, unity gain frequency around 1 GHz, and sampling capacitance (which is used for modeling the \( kT/C \) noise) equal to 1 pF. The resulting simulated output spectrum, reported in Fig. 8, shows that it is possible to achieve more than 14 bits of resolution with a signal bandwidth of 10 MHz. The noise floor present in the signal band is due to the \( kT/C \) noise contribution.

In order to verify the effect of capacitive mismatches on the performance of the proposed \( \Sigma \Delta \) modulator, we performed a statistical analysis, introducing random normally distributed coefficient errors with zero mean and standard deviation \( \sigma = 5 \cdot 10^{-3} \). The results achieved over 100 simulations, as shown in Fig. 9, demonstrate the robustness and the effectiveness of the used topology and are in line with the performance of low-sensitivity, high-resolution bandpass \( \Sigma \Delta \) modulators [6].

### V. Transistor-Level Simulation Results

The modulator is implemented at the transistor level using a 0.18-\( \mu \)m CMOS technology and a voltage supply of 1.8 V. The
opamps are designed using a two stages architecture with RC compensation. the comparators consist of a pre-amplification stage and a latch, while the DACs are resistive strings. the implemented opamps meet the specifications derived from the behavioral analysis (DC gain equal to 1000, slew-rate equal to 500 V/µs, and unity gain frequency equal to 1 GHz). fig. 10 shows the output spectrum of the MASH architecture implemented and simulated at transistor level, using the same conditions of section IV. the obtained SNR is about 80 dB with a signal bandwidth of 10 MHz, leading to an effective number of bit (ENOB) equal to 13.09. the SNR degradation with respect to the value obtained in fig. 8 is mainly due to switch and DAC non-idealities. Tab. I summarizes the power consumption of the circuits used in the modulator. the total power consumption is about 90 mW. For bandpass ΣΔ modulators, a useful figure of merit is defined as [4]

\[ FoM_{BP} = \frac{P}{2^{\text{ENOB}} \cdot 2 \cdot B \left( 1 + 3 \cdot \frac{\text{IF}}{f_s} \right)} \]

where \( P \) is the power consumption, \( B \) is the signal bandwidth, and \( f_s = F_s/2 \). The above is just a reasonable definition that accounts for the extra power needed by very high signals speed. The resulting FoM_{BP} for the proposed ΣΔ modulator is 0.15 pJ/conversion-level, which is well below the state of the art.

**ACKNOWLEDGMENT**

The authors wish to thank the FIRB (Italian National Program) Project RBAP06L455 for partial financial support.

**REFERENCES**


