Double-Sampling Analog-Look-Ahead Second Order $\Sigma\Delta$ Modulator with Reduced Dynamics

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Abstract—A double sampled second order $\Sigma\Delta$ modulator with an analog look ahead (ALA) approach is presented. The proposed architecture provides an extra clock period to be used for the quantization. The feedforward path in both integrators allows the further reduction of the output voltage swing, relaxing also the slew-rate requirements of the op-amps. Moreover, the modulator enables the reduction of the number of quantization levels in the quantizer, thus the overall power consumption of the modulator would be significantly reduced. The proposed solution has been simulated at behavioral level by considering an improved model which takes into account the slew-rate and bandwidth limits.

I. INTRODUCTION.

Portable communication systems require wide-band data converters with medium resolution and very low power. The $\Sigma\Delta$ technique is a suitable choice especially with multi-bit DACs that relax the noise shaping requirements. The order of the modulator, the number of bits of the quantizer and the oversampling ratio are the elements that the designer considers for a minimum power consumption. Furthermore, the modulator can be continuous-time or sampled-data. There are advantages and disadvantages for both solutions. The most relevant benefit of continuous-time is the low power but the noise caused by the clock jitter is a significant limit for very high clock frequencies. Besides, the linearity of the DAC can be a significant source of noise and distortion. Therefore, for medium and high resolution it is prudent to use the sampled data method but the power cost must be carefully considered.

As is known the double sampling technique enables the doubling of the sampling frequency with a negligible extra cost in the op-amp power consumption. This is quite effective for $\Sigma\Delta$ schemes because the number of bits is increased by the order of the modulator plus one. The double sampling method avoids the phase during which the op-amp does not integrate charge and actively operates the op-amp during both phases. Since input and output must be sampled by two different capacitors it is necessary to reduce the effect caused by mismatch but suitable proposed techniques moderate the limit. Indeed, a suitable time-slot for the quantizer must be allocated. In conventional $\Sigma\Delta$ schemes this time is the half of the full period delay unused by the last integrator. Since with double sampling scheme the integrator uses the full period, the time necessary for quantization must be borrowed from the full period. This increases the power of the integrator and the power of the ADC.

This paper describes a design method that provides an extra clock period to be used for the quantization. The method, called Analog Look Ahead (ALA), combined with a significant reduction of the slew-rate requirements of the op-amps enables conversion with a relatively high oversampling ratio (OSR) and low power.

II. IMPACT OF DYNAMICS IN THE POWER CONSUMPTION.

The power needed for the operation of a sampled-data $\Sigma\Delta$ modulator is mainly the power of the op-amps (or OTAs) and the ADC. The power of the digital sections is normally negligible. An effective conversion of wide-band signals seeks for the maximum OSR permitted by technology, while using a given order of the modulator and a reasonable number of bits in the quantizer. However, increasing the clock frequency increases the power because of the request of op-amp bandwidth and slew-rate. Consider, for example, a conventional modulator running at 320 $MHz$ and 1 $V_{FS}$. The time for integration is 1.56 $ns$. Simulations with a behavioral model show that the slewing time must be lower than 0.2 the available time. Therefore, with a full swing signal and a small capacitance like 0.2 $pF$, the bias current of the input differential pair must be

$$I_B = \frac{\Delta V}{\Delta t} C_{eq} = \frac{0.2 \cdot 10^{-12}}{0.2 \cdot 1.56 \cdot 10^{-9}} = 640 \mu A \quad (1)$$

Supposing to have an overdrive of the input pair of 0.2 $V$ the estimated $f_T$ is about 2.5 $GHz$, more than enough for medium resolution. Therefore, being the slew-rate the limit to low power it is necessary to use architectures that reduce the voltage swing of integrators. In addition, a limited voltage swing enables the use of power effective schemes like the telescopic cascode.

![Fig. 1. Second order $\Sigma\Delta$ modulator with feedforward paths](image-url)
The error caused by a limited speed of the OTA used in the second stage is less relevant than the one of the first stage because it is shaped at the first order. As a rule of thumb we can suppose that the current bias of the input pair can be half the one of the first stage OTA.

The above considerations have been verified by a behavioral model, improved with respect to the one described in [1]. This new model takes into account the slew-rate and the finite bandwidth limits. The simulations were done achieving the same SNR, for a traditional second order architecture and the one with the forward loops (Table I). The modulator of Fig. 1 shows the feedforward paths at the input of the second integrator and the quantizer. With this comparison, for the single and double sampling cases, it is possible to emphasize the benefits of reducing the signals swing for the power reduction. The estimated power consumption of the OTA’s given in Table I for a 1.5 V power supply assumes that the power is dominated by the input stage. Actually, unless using a telescopic scheme, there is an additional consumed power; therefore, for a quantitative estimation it is necessary to refer to the specific OTA architectures. However, as Table I shows, the power reduction can be as large as 3 times if both output swings are less than the input pair overdrive (assumed in the behavioral model 0.2 V).

Supposing to reduce the power by significantly limiting the output swing, the power is determined by the needed \( f_T \) that, for medium resolution is 2–3 times the clock frequency. Under these conditions the double sampling technique is very convenient because the integration time doubles and the needed \( y_m \) halves. This reduces by approximately 4 times the bias current (see the current in the first integrator for the traditional single sampled and the feedforward double sampling topologies).

### III. ANALOG LOOK AHEAD

For double sampled analog \( \Sigma \Delta \) modulators, the use of the full period for the signal integration does not leave any time for the quantization and requires possible modifications of the modulator architecture for relaxing the feedback timing. This discussion is treated in a recent publication [2]. It uses extra branches in the architecture that obtain an extra delay available for the quantizer and therefore the double sampled integration can be done in the complete half cycle. However, the solution requires an extra delay of the input signal that complicates the circuit implementation. This paper obtains the same result with a different approach, called Analog Look Ahead (“ALA”) \( \Sigma \Delta \) modulator.

#### A. The Analog Look Ahead principle

In order to explain the method let us start from the single-loop second order architecture shown in Fig. 2. The system obtains an extra clock period if the input of the quantizer is the anticipation of the voltage granted at the output of the second integrator, \( P_2 \), during the next clock period. This, by inspection of the diagram of Fig. 2 is

\[
P_2(n + 1) = P_2(n) - 2Y(n) + 2P_1(n) \tag{2}
\]

that in the \( Z \) domain becomes

\[
P_2(z) = z^{-1} (P_2(z) - 2Y(z) + 2P_1(z)) \tag{3}
\]

and therefore, a full clock period delay becomes available for the \( A/D \) and \( D/A \) conversion. The prediction in equation (3) can be realized with the architecture shown in Fig. 3.

The method can be extended to any \( \Sigma \Delta \) architecture to obtain an extra clock period delay for the quantizer. The cost of the method is an additional processing in front of the
quantizer. The operation can be done with a passive network if the number of comparators used by the flash A/D is low (i.e. not more than 5). For many comparators it is necessary to use an extra OTA within a zero delay scheme.

B. The proposed dynamic reduction ALA ΣΔ modulator

The proposed ALA topology gives the advantage to enable complete clock periods for the injection of the signal at the input of integrators. Moreover there is a complete clock cycle for the quantization of the second integrator that is sampled at the end of the full injection period. These features enable the double sampled ΣΔ schemes whose architectures use in each integrator a pair of switched capacitor inputs working in ping-pong fashion.

As discussed above, doubling the injection time significantly relaxes the OTA specifications but there is another important feature: to have a low output swing in the OTAs. If it is below the overdrive of the input pair there is no slewing and the full clock period is used for the exponential settling of the output voltage (supposing a single pole transfer function). Therefore, in addition to double sampling capability it is necessary to use architectures that give rise to small outputs.

The two feedforward of Fig. 1 reduce the voltage swing of both OTA’s. These additional branches can be added to the scheme with the ALA addition. Since the first feedforward enters the input of the first integrator, it is necessary to add an extra injection to the ALA equal to the input multiplied by 2x. The second feedforward can be done directly at the input of the ALA giving a total extra term of 3x the input signal, as is shown in Fig. 4.

Another element critical for the power consumption is the flash. Its power depends on three factors: the quantization amplitude, the conversion rate and the number of comparators. The quantization amplitude, ΔQ, multiplied by the preamplifier transconductance gives the current that charges the parasitic capacitance, Cp, of the latch. Supposing that the latch requires a minimum voltage signal ΔVmin the charging time

\[ \Delta t = \frac{\Delta V_{min} C_p}{g_m \Delta Q} \tag{4} \]

must be a fraction of the clock period. Therefore, since increasing gm requires a quadratic increase of the bias current, the number of bits of the quantizer must be carefully chosen.

According to simulations, 3 or 4 bits are the best trade off with a converter full range of (0.5–1) V.

For a given flash resolution and medium OSR the power consumption of the flash can be reduced by observing that the dynamic range at the output of the ALA stage in Fig. 4 is the digital output minus the quantization error. This is the full scale (or more for 0dB inputs) and requires to use \((2^N - 1)\) comparators for the quantization. It is possible to reduce the number of required quantization levels by exploiting the correlation between two successive samples granted by the oversampling (see Fig. 5) [3]. The amplitude of \(P_2(n) - Y(n-1)\) is smaller than \(P_2(n)\); therefore quantizing \(P_2(n) - Y(n-1)\) reduces the number of comparators of the flash A/D. The extra branch of Fig. 5 added to the already existing ALA input of \(-2Y\) gives a total injection of \(-3Y\). A topological transformation that moves the gain by 2 of the integrator at the input of the quantizer gives the proposed analog double sampled look ahead ΣΔ modulator shown in Fig. 6. The reduced dynamic ranges in the integrator’s outputs and the reduced quantization levels are obtained because of the prediction realized in the ALA stage.

Notice that the extra delay for the quantization is obtained without the necessity of analog delays in the forward paths. As a result, the architecture can be designed with a switched capacitor implementation. The forward paths addition can be realized at the input of the second switched-capacitor integrator and in the ALA stage, respectively. The ALA stage can be implemented with a switched capacitor summation circuit [4] at the input of the quantizer and another operational amplifier (or OTA) is not necessary.

The digital operations which make the reduction of the quantization levels in the flash A/D converter barely increase the area and power consumption. The reduction of the signal dynamics within the ALA ΣΔ modulator gives the possibility to use operational amplifiers with relaxed characteristics.
TABLE II
SIMULATION RESULTS OF THE PROPOSED DOUBLE SAMPLED ALA ΣΔ

\[ SN_{R_{\text{ideal}}} = 68 \text{ dB} @ -1 \text{ dB}, F_s = 320 \text{ MHz} @ OSR = 16 \]
\[ C_L = 0.2 pF, \text{ Overdrive Voltage: 200 mV} \]

<table>
<thead>
<tr>
<th>Architecture</th>
<th>( I_{\text{max}} ) 1st int. (μA)</th>
<th>( I_{\text{max}} ) 2nd int. (μA)</th>
<th>Tot. power (mW)</th>
<th>SNR</th>
<th>Bit</th>
<th>Comparators</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time relaxed [2]</td>
<td>80</td>
<td>60</td>
<td>0.21</td>
<td>67.1</td>
<td>3</td>
<td>7</td>
</tr>
<tr>
<td>ALA (this work)</td>
<td>61</td>
<td>78</td>
<td>0.20</td>
<td>67.0</td>
<td>3</td>
<td>4</td>
</tr>
</tbody>
</table>

![Power spectrum](image1)

**Fig. 7.** Power spectrum

**III. SIMULATION RESULTS**

The analog look ahead ΣΔ modulator was simulated in Matlab Simulink with an improved model for the discrete time integrators. This new model takes into account the finite bandwidth of the operational amplifiers and the slew-rate condition for the double sampling technique. In order to find the position of the proposed architecture on the state of the art in analog ΣΔ modulators, the simulation results are compared under the same conditions with one of the most recent architectures reported [2]. Fig. 7 shows the power spectrum of the double sampling ALA ΣΔ modulator for several cases. The input signal is set close to the Nyquist limit where the sampling frequency is 320 MHz. The SNR is almost equal to the ideal value with a current in the input transistors equal to 61, μA and 78 μA respectively (the swing in the second OTA is higher). Lowering the current supply a 20% reduces the SNR by 3 dB (see Table II). The relaxed feedback timing ΣΔ modulator has a similar signal dynamic behavior for the first and second integrators and the slew-rate limits are similar to the proposed ALA technique. On the other hand the ALA architecture yields a reduced input dynamic in the quantizer. This is traduced in a reduction in the number of quantization levels and so in the number of comparators needed in the flash A/D converter. The quantizer input for the proposed double sampling ΣΔ modulator and the double sampling time relaxed architecture [2] are compared in Fig. 8. The principal characteristics are summarized in Table II.

![Input Voltage Swing Quantizer](image2)

**Fig. 8.** Comparison of input voltage swing of quantizer.

**IV. CONCLUSION**

A new analog look ahead second order ΣΔ modulator was proposed. The architecture reduces the integrator’s output signal swing as well as the quantization levels in the flash A/D converter. This method grants an extra delay for the double sampling technique and the integration can be realized in the whole clock period. Simulations that account for the slew-rate and finite bandwidth in the operational amplifiers (or OTA’s) verify the method. Since with 3 bits the number of necessary comparators is only 4 the ALA can be implemented with a passive network without significant extra power.

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**REFERENCES**