Gain Enhancement Technique for High-Speed Switched-Capacitor Circuits

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ABSTRACT

This paper presents a novel technique for the compensation of the finite gain in active stages used in SC circuits. Simulation results are provided which show a good reduction in both module and phase errors. This technique is a good candidate to be used in high speed SC circuits where the need for a high gain-bandwidth imposes the use of low gain active stages.

I. INTRODUCTION

Switched capacitor (SC) techniques compete with Digital Signal Processing (DSP) in the audio band; they are normally used only for simple and low cost applications, DSP being more effective for more complex structures. However, recent technological improvements make it possible to greatly increase the speed of analog circuits, hence allowing a significant band increase in sampled data analog signal processors. At present, advanced CMOS technologies allow the processing of signals whose bandwidth is in the range of tens of MHz.

The key problem is to obtain high accuracy; in this respect, the main limitation in sub-micron devices is the degradation of the output resistance because of short channel effects. Instead of op-amps, SC circuits use OTA’s with voltage gain given by the product of the transconductance and the output resistance ($g_m R_0$). Thus the bandwidth increase resulting from advanced technologies is counterbalanced by a significant gain decrease. Now we have to remember that the error in analog processors is inversely proportional to the finite gain of the active elements and that it cannot be corrected with postprocessing digital techniques. In order to overcome the performance degradation, a number of circuit techniques have been proposed. All of them achieve a partial compensation of finite gain effects [1]–[4]. Some of them improve the gain (module) error, while others are more effective in compensating the phase error. This paper proposes a novel compensation technique which leads to a considerable reduction in both module and phase errors. The good performance of the proposed technique is demonstrated by circuit analysis and computer simulation.

II. PRELIMINARY CONSIDERATIONS

Most of the present finite gain compensation techniques are based on methods which can be called "predict and correct". Due to the finite gain $A_0$ of an operational amplifier, the inverting input does not behave as a perfect virtual ground, but shows a voltage displacement equal to $-\frac{V_0}{A_0}$ ($V_0$ is the output voltage). The errors (both module and phase) are reduced if the virtual ground displacement is predicted and corrected with a suitable additional circuit.

The switched capacitor technique is particularly suitable for implementing predict and correct methods. Since it is a sampled data technique, it is possible to perform prediction during one phase and to correct the operation of the circuit during the other. However, the input signal used for the prediction is not, in general, the same used for the correction. Therefore, even if errors depend on the specific circuit used, they normally degrade when the signal frequency is increased [1], [2]. For very high Q applications the output signal is very close to a sinewave; therefore, for the prediction phase we can use the information from the previous period. This requires suitably memorizing signal samples and using an integer ratio between the clock and the center frequency [3]. Another solution is to hold the input signal over the entire clock period making it necessary to use three clock phases [4].

In this paper we propose a novel scheme which performs prediction and correction of the finite gain error simultaneously. It does not require extra clock phases and does not introduce any delay between input and output. Moreover, as we will see in the following, the error corrections are superior to presently used techniques.

III. PRINCIPLE OF OPERATION

Fig. 1 shows the basic idea proposed in this paper. It is illustrated for a simple SC active circuit with a generic SC network connected in feedback and another connected between the input terminal and the virtual ground. These SC networks are represented by their charge/voltage transfer functions $Y(z) = \Delta Q / V$ [5].
OTA2 comprises two input pairs: (M1, M2) controlled by the voltage of the virtual ground of OTA2 (v1) and (M3, M4) controlled by the voltage of the virtual ground of OTA1 (v1'). By symmetry, OTA1 is made of an equal input structure with (MS1, MS2) grounded.

IV. CIRCUIT ANALYSIS

From the circuit in Fig. 1, using the conceptual equivalence between the charge/voltage transfer function of an SC network and the admittance of a continuous-time network, we can write the following equations in the z-domain thus:

\[
\begin{align*}
(Y_{in}(z) - V_1'(z)) Y_1(z) &= (V_1'(z) - V_0'(z)) Y_2(z) \\
V_0'(z) &= -A_1 V_1'(z) \\
(V_{in}(z) - V_1(z)) Y_1(z) &= (V_1(z) - V_0(z)) Y_2(z) \\
V_0(z) &= -A_2 V_1(z) + A_3 V_1'(z)
\end{align*}
\]  

(1)

where \( A_1 = 1 / R_0 \), \( A_2 = \beta_{m2} / R_0 \) and \( A_3 = \beta_{m3} / R_0 \). Writing (1) we assumed that \( V_1'(z) = Y_1(z) \) and \( V_2'(z) = Y_2(z) \). This is fully justified by the good matching of integrated capacitors. By routine analysis, we obtain:

\[
H'(z) = \frac{Y_0'(z)}{V_{in}(z)} = -\frac{Y_1(z)}{Y_2(z)} \left( \frac{1}{1 + \frac{Y_1(z)}{Y_2(z)}} \right)
\]  

(2)

\[
H(z) = \frac{V_0}{V_{in}} = -\frac{Y_1(z)}{Y_2(z)} \left( \frac{1}{1 + \frac{Y_1(z)}{Y_2(z)} + A_1 - A_3} \right) \left( 1 + \frac{A_2 + A_3 + \frac{Y_2(z)}{Y_1(z)+Y_2(z)} A_1 A_2}{A_1 A_2} \right)
\]  

(3)

for the uncompensated and compensated transfer functions, respectively.

By inspection of (2) and (3), we can observe that the two denominators, showing the errors, have a dependence on I/A
and }1/A^2\text{ respectively. This is a rough but clear indication of error reduction.}

V. THE GAIN ENHANCED INTEGRATOR

To apply the previously derived equations, we now analyze the inverting SC integrator and estimate the module and phase errors. Fig. 3 shows the proposed gain enhanced integrator. Equations (2) and (3) become:

\[
H'(z) = \frac{H_i(z)}{1 + \frac{\alpha z + z - 1}{A_1}}
\]

\[
H(z) = \frac{H_i(z)}{1 + \frac{\alpha z + z - 1 + A_1 - A_3}{A_2 + A_3 + \frac{z - 1}{\alpha z + z - 1} A_1 A_2}}
\]

where } \alpha = (C_1 / C_2) \times 1 \text{ and } H_i(z) = -\alpha z / (z - 1) \text{ is the transfer function of the ideal integrator. Substituting } z = e^{j\omega T} \text{ in (4) and (5) and following the derivation given in [6], we can write a generic transfer function in the form:}

\[
H(e^{j\omega T}) = \frac{H_i(e^{j\omega T})}{1 - m(\omega) - j\theta(\omega)}
\]

where } m(\omega) \text{ and } \theta(\omega) \text{ are the magnitude and the phase errors. From (4) and (5), after some calculations, we find for the uncompensated circuit:}

\[
\begin{align*}
\{ m'(\omega) &= \frac{A_1}{1 + \frac{\alpha}{2}} \\
\theta'(\omega) &= \frac{\alpha}{2 A_1 \tan \frac{\omega T}{2}}
\end{align*}
\]

and for the compensated circuit:

\[
\begin{align*}
m(\omega) &= \frac{\alpha}{2 + \alpha + \Delta A} \left( \frac{\alpha}{1 + \frac{\alpha}{2}} \right) \left( \frac{\alpha}{1 + \frac{\alpha}{2}} \right) \left( \frac{\alpha}{1 + \frac{\alpha}{2}} \right) \left( \frac{\alpha}{1 + \frac{\alpha}{2}} \right) \left( \frac{\alpha}{1 + \frac{\alpha}{2}} \right) \left( \frac{\alpha}{1 + \frac{\alpha}{2}} \right) \\
\theta(\omega) &= \frac{2}{\alpha \left( 1 + \frac{\alpha}{2} \right) \tan \frac{\omega T}{2}}
\end{align*}
\]

where we defined } \Delta = A_1 - A_3, \Sigma = A_2 + A_3, \Pi = A_1 A_2 \text{ and } \Omega = \omega T / 2.

Under the hypotheses } A_1 = A_2 = A_3 = A, \omega T = 1 \text{ and } \omega T / \alpha = 1 \text{ (that is around the integrator unity gain frequency), equation (8) is approximated by:}

\[
\begin{align*}
m(\omega) &= \frac{\alpha}{\alpha^2} \\
\theta(\omega) &= \frac{2}{\alpha^2}
\end{align*}
\]

showing an improvement by a factor of about } 1/A \text{ with respect to the uncompensated circuit (equation (7)). With a mismatch } \Delta A \text{ between the three voltage gains, we have:}

\[
\begin{align*}
m(\omega) &= \frac{\alpha + \Delta A}{\alpha^2} \\
\theta(\omega) &= \frac{2 + \Delta A}{\alpha^2}
\end{align*}
\]

VI. SIMULATION RESULTS

The previously described circuit was analyzed by computer simulation. The following conditions apply: } A_1 = A_2 = A_3 = 100, C_1 / C_2 = 0.2, f_c \text{ (sampling frequency) } = 10 \text{ MHz and } f_T \text{ (unity gain frequency) } = 318 \text{ kHz (modern technologies permit clock frequencies as high as 10 MHz). Fig. 4 shows the magnitude and phase errors for the compensated and the uncompensated integrator calculated by means of circuit simulation.}

In the band around the unity gain frequency, we have a lower than 0.001 dB magnitude error, which is better than the performance provided by the solutions proposed in [1] (= 0.02 dB) and in [2]. The phase error is } 0.01 \text{ degrees, which is in the same order of magnitude as the best solution shown in [2].}

Fig. 5 accounts for mismatches of } g_{m3} \text{ with respect to } g_{m1} \text{ in the range } \pm 4\%. This range is well beyond what can be expected in integrated realizations. Nevertheless, the gain
error is confined within a few milli dB. Similar performance is found in mismatches of the output resistances. As expected from (8) the mismatch of $gm2$ with respect to the other transconductances is substantially irrelevant.

VII. CONCLUSIONS

We have presented a novel approach for the compensation of the finite gain in active stages used in SC circuits. The analysis given and the results of computer simulations showed a good reduction in both gain and phase errors; globally better than the solutions until now proposed.

The proposed method allows us to use, even in high accuracy SC circuits, gain stages with gain as low as 40 dB or less. The good results achieved are paid for by an increase in chip area and by nearly doubling power consumption.

![Graph A](image1.png)

![Graph B](image2.png)

Fig. 4 - Comparison of magnitude (a) and phase (b) errors between:
(i) uncompensated SC integrator;
(ii) compensated SC integrator.

![Graph C](image3.png)

Fig. 5 - Magnitude (a) and phase (b) errors of the compensated SC integrator in the presence of mismatches between $gm3$ and $gm1$.

REFERENCES


