Design issues on high-speed high-resolution track-and-holds in BiCMOS technology

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Abstract: The authors address some fundamental issues in track-and-hold (T&H) design. A number of explicit expressions characterising the main limitations of this class of circuits are given. A fully differential open-loop T&H is presented satisfying the stringent specifications imposed by present telecom applications. It exhibits high-resolution (12 bit) and high-speed ($f_c > 160$MHz) as measured on samples integrated in a standard 0.8μm 12-GHz BiCMOS technology. The overall performance is beyond state-of-the-art. The T&H's size is 0.37mm$^2$, and it consumes 45mA from a 5V power supply.

1 Introduction

The evolution in radio communication systems has been towards increasing complexity and, at the same time, wider flexibility [1]. Consequently, the most suitable approach has been to digitise the analogue signal as soon as possible and to devolve all the processing to DSP, which can be easily reconfigured via software. However, the new telecom architectures foreseen for this task provide challenging specifications for A/D converters, by requiring high-speed ($f_c > 100$MHz), high resolution (12-14 bit) and linearity (spurious free dynamic range, SFDR $<-97$dB).

Although it is possible to implement complex algorithms to digitally correct the internal blocks of an ADC, the bottleneck in the conversion system is the input T&H, whose non-idealities cannot be compensated by computations.

A variety of T&Hs have already been presented, dealing with different targets: very high-sampling-rate low-resolution [2-4], high-sampling-rate low-voltage medium-resolution [5, 6], high-sampling-rate high-resolution [7-14]. This work focuses on the last class, by examining the main limitations both in frequency and precision and deriving explicit analytical expressions. Starting from these, the structure and building blocks of a 12-bit 160MHz track-and-hold realised in a 0.8μm BiCMOS technology are described together with extensive experimental results.

2 Track-and-hold principle

The logical block diagram of a track-and-hold is shown in Fig. 1. We distinguish three sections: the input buffer (IB), the sampler (SMP) and the output buffer (OB). The main purpose of the IB is to decouple the signal source and the sampling section, whose input capacitance can be quite high. This function must be performed without introducing distortion and with suitable speed. The simplest buffer can be realised using a MOS follower (level-shifter). However, the distortion introduced by PMOS or NMOS devices is very high: the transconductance is lower than the bipolar counterpart and the body effect affects the threshold of MOS devices if their body cannot be shorted to the source. Therefore, it is better to use bipolar transistors instead. To assess the possible accuracy, we calculate the expected distortion when a BJT level-shifter drives a capacitance $C_s$.

$$$$
where $V_{be}$ is the thermal voltage, $V_p$ is the signal peak amplitude, $f_n$ is the input frequency, $C_s$ the sampling capacitance and $I_{b1}$ the level-shifter bias current. For example, using $I_{b1} = 2$mA, $C_s = 5pF$, $f_n = 100$MHz, $V_p = 0.25V$, a distortion of at least -66dB is obtained.

$$$$
Eqn. 1 establishes also a relation between the gain-bandwidth product of the level-shifter and the expected distortion. Considering that

$$GBW = \frac{I_{b1}}{V_T} \frac{1}{2\pi C_s}$$

we have:

$$HD_3 = 20 \log \left[ \frac{1}{12} \left( \frac{V_p}{V_T} \right)^2 \left( \frac{f_n}{GBW} \right)^3 \right]$$ (2)

Fig. 1 Track-and-hold principle
Eqn. 2 fixes a lower limit for the GBW if very low harmonic distortion is needed. For example, using the above figures, to achieve HD3 = -84dB, the GBW must be at least 5GHz.

Let us consider now the sampling and hold operations (SMP). The simple implementation shown in Fig. 1 uses a MOS switch and a capacitor. However, the nonlinear behaviour of the \( r_c \) resistance with \( V_{ce} \) and the nonlinear clock-feedthrough limit the distortion performance of the sampler. Therefore, once again, BJT-based solutions should be preferred.

For any circuit implementation, another important source of imperfection is the so-called 'aperture error'. The non-zero time over which the T&H disconnects from the input is the so-called 'aperture time' \( t_A \). Since \( t_A \) generally depends on the instantaneous slope of the input signal, variations produced in it, i.e. \( \Delta t_A \), cause an aperture error.

It, in turn, introduces distortion to the held samples. For conventional T&H topologies [lo], the typical \( \Delta t_A \) modulation does not guarantee an equivalent linearity better than 10 bit.

The last block in Fig. 1 is the output buffer OB. It exhibits distortion and settling limitation, similar to those in the IB. In addition, we have to account for the droop effect. It results from discharging currents in the hold phase. If the discharging currents are a nonlinear function of the signal, a distortion is produced. As shown in Fig. 1, \( R_p \) represents the input impedance of the OB. If \( R_p \) is linear, the voltage on \( C_s \), after an hold period of \( T \) becomes:

\[
V_{C_s}(T) = V_{C_s}(0) \left(1 - e^{-T/(R_p C_s)}\right) - \frac{I_{\text{leak}} T}{C_s}
\]

That would cause an offset error and a gain error. Unfortunately, with bipolar emitter followers, the input impedance is \( R_p = r_c + R_{ne} \), where \( R_{ne} \) is a nonlinear function of \( V_{ce} \). Therefore, the droop rate error becomes a nonlinear function of the input voltage. In turn, harmonic distortion appears.

In addition to the above non-idealities we have also to consider other spur sources. Among them are the thermal noise. Since the thermal noise of active devices is inversely proportional to \( g_{m} \), the use of bipolar devices with large bias current and low intrinsic base resistance is recommended. A second source of possible performance degradation is the clock jitter. It causes a sample-to-sample variation in time between the effective points at which the samples are actually taken. Clock jitter is often due to phase jitter on input signals or unwanted phase-modulation of the sample clock by random noise, supply line noise or digital noise caused by an inaccurate physical layout. By considering a 'white noise model', the SNR can be expressed by [15]:

\[
SNR_{\text{AB}} = 20 \log \left(\frac{1}{2\pi f_{\text{fmax}} I_{u,RMS}}\right)
\]

where \( I_{u,RMS} \) is the root mean square value of the jitter (assuming a Gaussian distribution). To obtain a SNR equivalent to 12 bits with a 100MHz input signal, a \( I_{u,RMS} \) lower than 0.32\( \mu \)s is needed. From the above considerations, it seems that if we deal with a BiCMOS technology it is preferable to use bipolar devices in all signal paths, while the presence of MOS could guarantee good upper current mirrors and a better droop rate.

3 Conventional track-and-hold structures

This paragraph considers two track-and-hold structures published in the literature and compares their perform-
Q_{out} remains off with any possible input signal. With a typical signal of $V_i = 0.25\text{V}$, we achieve the required drop with $R = 100\Omega$ and $I_b = 2.5\text{mA}$. These figures are acceptable even if the circuit can suffer by some speed limitation.

At high frequency the implementation in Fig. 5 suffers of the following limitation: the inverse current-to-voltage conversion performed by the series $Q_1$-$R_5$ and $Q_T$-$R_4$ only partially corrects the nonlinearity of the input pair $Q_1$-$R_1$ and $Q_2$-$R_2$. At very high frequencies possible mismatches of relative delays critically affect the expected compensations.

In addition, the clock rate is limited by the time constant due to $R_1$ and $R_4$ and the parasitic capacitance at nodes A and B. An evolution of this topology proposed by [14] overcomes some limitations. However, since it makes use of an IB similar to that in Fig. 5, it suffers from the same problems at high frequencies, which limits its resolution to $10\text{bit}$.

A final point to keep in mind concerns the voltage of nodes A and B in the hold mode. The extra-currents $I_b$ flow through the input buffer loads and pull down the voltage of A and B as required. However, their value can be so low as to bring transistors Q1 or Q2 into the saturation region.

Fig. 4  Simplified schematic diagram of switched emitter follower

Fig. 5  Schematic diagram of SEF proposed in [8]

Fig. 6  Schematic diagram of SEF proposed by authors

Fig. 7  Input buffer with non-ideal current sources

4 New track-and-hold topology

We have seen in the previous Section that the SEF architecture is better than the diode bridge, especially when our key goal is high resolution. However, it is possible to improve the SEF performances by using the ameliorating solutions that will be discussed in this Section. A first improvement results from the input buffer. Fig. 6 shows the circuit used. The signal at node A is a replica of the input because of the shift down of $Q_{in}$ (at node B) and the shift up of the diode connected element $Q_d$. Since the current in the two transistors is the same, the two level-
shifters match and possible nonlinearities are cancelled. Noted, in the hold mode, the current through Qo pulls down the voltage of node A until the clamping transistor Qclp turns on and fixes the voltage of node A one $V_{be}$ below the input. The diode connected transistor Qd is reversed biased. Therefore, we avoid the risk to push the input transistor $Q_{in}$ into saturation. The impedance driving down the voltage of node A until the clamping transistor $Q_{clp}$ are clamped at a fixed voltage.

Another general problem in T&H topologies is the so-called hold-mode feed-through (HMF). It is a perturbation of the hold signal due to imperfect insulation between the input and the output during the hold phase because of parasitic stray capacitances. In the implementation of Fig. 6, transistor $Q_{dp}$ has its base connected to $V_{be}$. During the hold phase a fraction of the signal appears at the output. It is due to the nonlinear capacitive divider $C_{y, out}$ and $C_y$. Therefore, the HMF is given by:

$$HMF = 20 \log \left( \frac{A_v C_{y, out}}{C_y + C_{y, out} + C_s} \right)$$

where $A_v$ is the gain of $Q_{dp}$ and $C_{y, out}$ is the intrinsic base-emitter capacitance of $Q_{out}$. For typical values $C_{y, out} = 1 \mu F$, $C_y = 10 \mu F$ and $A_v = 1$, it follows that the HMF is $-20 \text{dB}$. To circumvent this error, the solution in Fig. 8 presents a single-ended arrangement. Biases the base of $Q_{dp}$ with a replica of the hold signal. Actually, in the hold mode, node A is controlled by two paths, one through $Q_{dp}$ and the other through the parasitic capacitance $C_{y, clp}$ and $1/gm_{clp}$. Therefore, the hold-mode feed-through worsens at angular frequencies higher than $1/gm_{clp}$. For a typical technology we can assume $g_{m, clp} = 0.15 \mu S$, $gm_{clp} = 0.3 \Omega^{-1}$. Therefore, with an input frequency of 100MHz the HMF is as good as $-80 \text{dB}$. The proposed solution is equivalent to that in [14], but is realised in a simpler manner and with reduced current consumption. Hold-mode feed-through can be compensated with crossed feed-forward capacitors as proposed in [8]. That compensation technique is not very effective since it must rely on matching of nonlinear capacitances. Instead, the compensation approach used together with the replica of the hold signal further improves the HMF. This is achieved in the circuit of Fig. 9 that includes two feed-forward capacitors $C_f$ between node A (A) and B (B). $C_f$ is the series-parallel connection of four diodes [8], as shown at the bottom of the same Figure. The simulation results show an HMF as low as $-100 \text{dB}$. The unity gain buffer driving $Q_{dp}$ can generate kick-back noise that affects the output signal. The duplication of the SEF shown in Fig. 8 avoids this possible drawback. Actually, the hold capacitance of the auxiliary SEF is not connected to ground but to the degeneration resistance of the current source $I_p$. This connection dynamically changes
the value of $I_b$ during track mode, bootstrapping the current delivered to the sampling capacitance $C_s$. The qualitative result is that the modulation of $V_{pe}$ of $Q_{out}$ is reduced benefiting the harmonic distortion [11]. Using in our design $C_s = 8\mu F$ and $I_b = 8\mu A$, an improvement of about 10dB was obtained in THD.

Besides the harmonic distortion, the nonidealities in the track phase are related to settling and speed. Settling must be completed within a fraction of the track period ($\Delta T_T$) and this will demand a large bias current: during the hold interval ($\Delta T_H$) an input sine-wave may change by $V_{pp} \Delta T_H$. Therefore, with $V_{pp} = 0.25V$, $\omega = 2\pi 100M$rad and $\Delta T_H = 2.5ns$ (supposing a 200MHz clock rate), the SEF bias current should exceed 0.8mA/$\mu F$ to achieve settling within 1/5 of $\Delta T_T$.

The relationship of eqn. 10 leads to a strict limit on $R_{in}$ as $g_{m, out}/C_s$ (the bandwidth of the SEF) needs to be quite large to ensure minimum harmonic distortion. Let us assume $I_b = 2mA$, $r_{bb'} = 40\Omega$, $C_s = 10\mu F$, $C_{b'e,out} = 1\mu F$, the driving resistance $R_{in}$ must be lower than 25$\Omega$ to satisfy the relationship. This requirement contrasts with the need for a suitable voltage drop to guarantee $Q_{out}$ is turned off in solution [8]. Instead, the proposed solution exhibits a low output impedance ($2g_{out} = 20\Omega$), which avoids ringing.

The final output buffer (Fig. 11) drives the capacitance of the following circuitry. It has a single stage local-loop structure similar to the input buffer. However, its input impedance is enhanced by bootstrapping the collector-emitter resistance of $Q_4$, $r_{bb}$.

A simple circuit (shown in the same Figure) compensates for the input transistor common-mode base current. Transistors $M_{b1}$ and $M_{b2}$ mirror the base current in $Q_4$ and inject it into the base of $Q_1$. Since the base current of $Q_4$ is the same as in $Q_1$, an ideally perfect compensation of the base current is achieved, reducing the common-mode voltage droop during the hold phase.
5 Experimental results

An experimental T&H (without compensation capacitances $C_p$) was fabricated using a 0.8μm double-metal double-poly BiCMOS technology and occupied a 0.37mm$^2$ area. The die includes two T&Hs for dynamic testing purposes, bandgap references and clock buffers. Its micrograph is shown in Fig. 12.

The sine wave at the output of a signal generator was filtered by means of a band-pass high-selectivity filter, split into differential signals by a balun transformer and applied to the circuit. The T&H outputs were fed to another balun transformer driving a spectrum analyser. For all measurements the load was 50Ω/10pF. Fig. 13a shows the output spectrum with a 77MHz, 1 $V_{pp}$ input signal with the circuit in track mode. The second harmonic achieved is -87dB below the fundamental one, while the third is not significant. In contrast to the simulations, where the third harmonic was dominant, the measurements indicate an higher second harmonic, due to imbalances between the positive and negative paths induced by T&H layout mismatches and external component nonidealities (transformers, filters, etc.). Fig. 13b reports the output spectrum under the same condition with a clock of 160MHz. The second harmonic was around -72dB below the fundamental one, while the third was lower than -76dB. It is important to note that in this test the entire output waveform was analysed, whereas when a front-end for the ADC is used only the held values of the output are to be considered. Since the waveform exhibited slewing at the beginning of the track phase, this measurement represented a worst-case condition for the harmonic distortion. Moreover, the fundamental had an amplitude of around -5dB because of the attenuation introduced by the output transformer. The graph in Fig. 14 illustrates the degradation of the total harmonic distortion as a function of the sampling frequency. At the maximum frequency (250MHz) we again achieved 10 bit resolution (THD = -61dB). The dependence of the distortion on the signal amplitude indicates that it becomes -74dB when the input signal is 0.5 $V_{pp}$ with the same clock rate. Fig. 15 reports the hold-mode feed-through spectrum when $f_{\text{cm}} = 77$ MHz and the input amplitude is 1 $V_{pp}$. We achieve a hold-mode feed-through rejection of -68dB (including the balun attenuation). Finally, the differential droop rate was limited to 122μV/ns, while the common-mode droop rate was 250μV/ns, which corresponds to an input current of $\approx 2\mu A$ for the T&H output stage.
Table 1 summarises T&H performance parameters. The current consumption for each T&H is 45 mA (including output buffers) operating with a 5 V supply.

**Table 1: Performance summary**

<table>
<thead>
<tr>
<th>Feature</th>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>12GHz BiCMOS</td>
</tr>
<tr>
<td>Pedestal error</td>
<td>&lt; 2 mV</td>
</tr>
<tr>
<td>Total harmonic distortion</td>
<td>-70 dB @ 77 MHz</td>
</tr>
<tr>
<td>Hold-mode feed-through</td>
<td>-68 dB @ 77 MHz</td>
</tr>
<tr>
<td>Analogue bandwidth</td>
<td>250 MHz</td>
</tr>
<tr>
<td>Max differential input signal</td>
<td>1 Vpp</td>
</tr>
<tr>
<td>Max sampling rate</td>
<td>250 MHz</td>
</tr>
<tr>
<td>Droop rate</td>
<td>122 μV/ns (@ 1 Vpp)</td>
</tr>
<tr>
<td>Load</td>
<td>50 Ω/10 pF</td>
</tr>
<tr>
<td>Current consumption</td>
<td>45 mA @ 5 V</td>
</tr>
</tbody>
</table>

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