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as a diversity receiving antenna to improve received signals in mobile communications systems.

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P. Nganjyanaporn and M. Krairiksh (Faculty of Engineering and Research Center for Communications and Information Technology, King Mongkut’s Institute of Technology, Ladkrabang, Bangkok 10520, Thailand)

E-mail: kkmenai@kmitl.ac.th

References


Switched-capacitor bandpass filter with quasi-continuous digital Q-factor tunability

J.L. Ausin, J.F. Duque-Carrillo, G. Torelli and E. Maloberti

A second-order switched-capacitor (SC) bandpass filter with very wide Q-factor programmability range, is presented. Although the Q-factor is controlled by digitally varying the effective sampling frequency of an SC branch, quasi-continuous programmability is provided. Experimental results from a 0.8 μm CMOS integrated prototype demonstrate the viability of the proposed technique.

Introduction: Many integrated systems require the use of high-selectivity (high-Q) analogue bandpass (BP) filters [1, 2]. In general, for the monolithic implementation of filters, switched-capacitor (SC) techniques offer important advantages over their continuous-time counterparts. However, silicon area requirements become excessive for high-Q applications, since the capacitance spread is of the order of a single pF, which must be decreased, which leads to large silicon area.

A second-order switched-capacitor (SC) bandpass filter with very wide Q-factor programmability range, is presented. Although the Q-factor is controlled by digitally varying the effective sampling frequency of an SC branch, quasi-continuous programmability is provided. Experimental results from a 0.8 μm CMOS integrated prototype demonstrate the viability of the proposed technique.

Q-factor programming technique: Fig. 1a shows the circuit schematic of the second-order SC BP section used in the presented design [3]. A positive-feedback SC branch (i.e. F) has been included around the second amplifier. This branch operates with non-overlapping clock phases denoted \( \phi_1 \) and \( \phi_2 \), respectively. Assuming, initially, that these phases coincide with the operating clock phases of the other SC branches \( \phi_1 \) and \( \phi_2 \), derived from a master clock \( \phi_m \) (which corresponds to the traditional clocking scheme in SC circuits), the Q-factor is given by

\[
Q = \frac{1}{F} \sqrt{\frac{AC(E+B)}{D}}
\]

where \( A \) and \( B \) are the coefficients of the second-order SC BP section.

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Notice that the filter selectivity can be controlled by means of the number of pulses \( p_1 \) during which the SC branch \( F \) is active in a time interval \( mT_s \), i.e. by its effective sampling frequency \( f_{sef} \). Obviously, \( p_1 \) must be set smaller than \( mT_s \) to ensure circuit stability. It is worth mentioning that process variations involved in monolithic SC filter implementation affect the nominal ratio \( E/F \). Therefore, for very low values of the denominator of (2) (i.e. for very high Q-factors) a Q-tuning scheme should be included not only to guarantee circuit stability but also to automatically tune the required Q-factor value. Fortunately, given the versatility and the fine-programming capability of the proposed technique, as will be shown next, this is assumed to cause no major problems.

The Q-factor programmability resolution can be increased without any appreciable cost if the number of active pulses \( p_1 \) (i.e. \( p_1 = 1, 2 \)) of the clock signal \( \phi_m \) is made different in two successive time intervals \( mT_s \), i.e. \( p_1 \) and \( p_2 \) in Fig. 1a, respectively. In these operating conditions, (2) is still valid but the equivalent programming index \( p_2 \) is \( (p_1 + p_2)/2 \), where \( 1 \leq p_2 \leq m \), and the effective sampling frequency \( f_{sef} \) is \( (p_1 + 2p_2)/2m \). Extending the above idea, at least theoretically, any value of effective sampling frequency \( f_{sef} \) of the SC Branch \( F \) and hence, any value of the Q-factor can be obtained by means of a simple logic section that provides an adequate clock signal \( \phi_m \). The general expression of \( f_{sef} \) is given by

\[
N_{eff,f} = \frac{f_{sef}}{M \cdot m} \sum_{i=1}^{M} p_i
\]

where \( p_i \) represents the number of active pulses of the SC branch \( F \) in the \( i \)-th time interval within a sequence of \( M \) time intervals \( mT_s \), (the pulse sequence has an overall repetition period equal to \( MmT_s \). It is
Experimental results: The SC BP filter in Fig. 1a along with a digital section to provide the necessary clock signals was fabricated in conventional double-poly 0.8 μm CMOS technology. The circuit was designed to operate with 3 V of supply voltage and a clock frequency $f_c$ of 1 MHz. The capacitor values, in terms of unit capacitor $C_u = 0.25 \text{ pF}$, are indicated in Fig. 1a (poly-to-poly capacitors were used). The ratio $E/F$ was set to 0.7. Hence, according to (2), the programming index $p_i$ can vary, ideally, from 1 to 0.7 m.

A single-stage cascode mirrored topology was adopted for the two op-amps. Complementary switches were used (aspect ratio $= 10.4 \mu\text{m}/0.8 \mu\text{m}$ for NMOS and PMOS transistors). The digital section consists of two major blocks, i.e., a programmable clock generator (PCG), which allows the possibility of dynamically reconfiguring the clock signal $f_1$, and two non-overlapping phase generators, so as to provide uniform clock phases $f_1$ and $f_2$ and periodical non-uniform clock phases $f_1^\prime$ and $f_2^\prime$.

Fig. 2 shows the measured SC BP responses for $m = 16$ and $M = 1$, when varying $p_i$ from 1 to 11. In this case, the maximum allowed $p_i$ value is 11. The value of $f_{\text{eff}}$ ranges from 62.5 to 687.5 kHz in steps of 62.5 kHz, and the central frequency is 17.4 kHz. The measured values of the $Q$-factor range from 0.53 ($p_i = 1$) to above 300 ($p_i = 11$).

As previously stated, the programmability resolution can be increased by selecting different values of the index $p_i$, within a sequence of $M$ time intervals $m_T$. Two simple programming strategies will be now presented. The digital section was initially programmed to operate with $m = 16$ and $1 \leq p_i \leq 8$. In the first interval $m_T$, the index $p_i$ was set to an appropriate value ($p_i < 11$), whereas in the remaining $(M - 1)$ intervals $m_T$, $p_i$ was set to $(p_i + 1)$. Thus, according to (3), the value of $f_{\text{eff}}$ is given by

$$f_{\text{eff}} = f_c \frac{p_i}{m} + f_c \frac{M - 1}{M \cdot m}$$

(4)

For any given value of $M$, the resolution due to the variation in $p_i$ is the same as before (i.e., $f_c/m$). However, the term $f_c (M - 1)/M m$ acts as a programmable offset, which provides a resolution increase. According to (4), the higher the value of $M$, the closer the value of $f_{\text{eff}}$ to $(p_i + 1) f_c/m$. The new values of $f_{\text{eff}}$ represent intermediate values between two consecutive values (corresponding to $p_i$ and $p_i + 1$, respectively) of the initial programming setting (i.e. $m = 16$, $M = 1$). The PCG was subsequently reprogrammed to obtain values of $f_{\text{eff}}$ slightly higher than $p_i f_c/m$. To this end, the indexes $p_i$ for $1 \leq i \leq M - 1$, were set to a value less than 11, while the last index $p_{1M}$ was set equal to $(p_i + 1)$. The value $f_{\text{eff}}$ is now given by

$$f_{\text{eff}} = f_c \frac{p_i}{m} + f_c \frac{1}{M \cdot m}$$

(5)

i.e. the higher the value of $M$, the closer the value of $f_{\text{eff}}$ to $p_i f_c/m$. Fig. 3 shows some of the measured frequency responses obtained with the above programming strategies. Dark lines correspond to the frequency responses with the three highest $Q$-factor values in Fig. 2 (i.e., $9 \leq p_i \leq 11$). The achieved resolution increase (light lines) is clear. Other programming strategies were also successfully evaluated.

Conclusion: A programming technique suitable for high-$Q$ SC bandpass filters, has been proposed. It is based on the individual control of the equivalent resistance of adequate SC branches by means of their effective sampling frequency. Experimental results demonstrated its efficiency to achieve a quasi-continuous $Q$-factor programmability range up to very high $Q$ values.

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J.L. Aush and J.F. Duque-Carrillo (Department of Electronics and Electrical Engineering, University of Extremadura 06071 Badajoz, Spain)
G. Torelli and F. Maloberti (Department of Electronics, University of Pavia, Via Ferrata 1, I-27100 Pavia, Italy)

References

Differential CMOS edge-triggered flip-flop with clock-gating
Y. Xia and A.E.A. Almaini

A non-redundant transition clock chain is proposed and applied to differential edge-triggered flip-flops. PSPICE simulation shows that compared to a recently published design the proposed circuit can save power when the switching activity of the input signal is <0.65. Power reduction can be as high as 86% when the input is idle.

Introduction: Low power techniques are essential in modern VLSI design due to the increasing density and size of VLSI chips and systems. Research shows that the power consumption of a clock system is one of the main sources of power dissipation, typically 20 to 45% of total chip power. Consequently, many ingenious techniques have been proposed recently to reduce the clock power of the flip-flops [1, 2]. Since differential flip-flops can play the role of amplifiers, they can be used to amplify a small voltage signal on a differential reduced swing bus and at the same time they can latch the data. Hence, research efforts have been directed at improving their perfor-