Integrated CMOS Magnetic Current-Mode Hall Microsystems

2nd Year PhD Activities Report 2012/2013

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Outline

Introduction and Motivation

Design and Simulation Analysis

Circuit Implementation

Test and Measurements

Conclusion And Future Work
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Introduction and Motivation

- Improve the signal to noise ratio in the Hall effect sensors by integrating the signal current over a given period of time
- Looking for new approach to design the sensor system with: Low Noise - Low Offset - Low Power - High Sensitivity

GOAL OF THIS PROJECT

- Model of the sensor in the Hall structure and Current-Mode configuration
- Design, Simulation, layout and Measurement of the Current-Mode Sensor and related readout circuits
SNAPSHOT AND KEY RESULTS

SNAPSHOT

System Architecture
- Introduction and Motivation
- Simulation
  - COMSOL
- VERILOG-A
- Schematic
  - Layout
  - Fabrication
- Test and Measurement
  - Sensors and Integrator

KEY FEATURES OF THIS PROJECT

- New Magnetic Hall Sensor based on Current-Mode approach that optimizes the sensitivity and resolution of the magnetic field.
- Use of current spinning technique to reduce offset and 1/f noise.
- Integrate the differential output currents by an integrator as a read-out circuit.
Conventional Voltage-Mode Hall Sensor Architecture

\[ S_V = G \frac{r_H}{qnt} \]
**General Description**

**Sensitivity**

\[ S_I = \frac{I_{Hall}}{I_{bias} B} \]

**Proposed Current-Mode Hall Sensor**

\[ I_{H+} = \frac{I_{bias}}{2} + \frac{I_{Hall}}{2} \]

\[ I_{H-} = \frac{I_{bias}}{2} - \frac{I_{Hall}}{2} \]

\[ I_{HP} = I_{H+} - I_{H-} = I_{Hall} \]

\[ I_{HN} = I_{H-} - I_{H+} = -I_{Hall} \]

The **difference of the output currents** is \(2xI_{Hall}\), thus doubling the sensor sensitivity with respect to the conventional implementation.
GENERAL DESCRIPTION

Current Spinning Technique

Four phases for current spinning method

Offset Reduction

Switches Circuit

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SIMULATIONS include:

- COMSOL Multiphysics
- VERILOG-A

GENERAL DESCRIPTION

New Hall structures in the COMSOL have been studied and compared the results to Verilog-A model in the Cadence environment for evaluating and optimizing the sensor with respect to noise, offset and sensitivity.
Simulation of output currents after four phases for current spinning method

Hall Plates in COMSOL Environment
An Equivalent Model Topology for The Hall Plate

Parameters:
1- external magnetic field (B)
2- initial value of resistors (R0)
3- magnetic resistance coefficient (β)

The 8-resistor Verilog-A model of Hall plate

<table>
<thead>
<tr>
<th>Magnetic Field</th>
<th>COMSOL</th>
<th>VERILOG-A</th>
</tr>
</thead>
<tbody>
<tr>
<td>B₀ [mT]</td>
<td>I_D[μA]</td>
<td>I_C[μA]</td>
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<tr>
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<td>6</td>
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<tr>
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<td>20</td>
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</table>
Circuit Implementation

The proposed microsystem, consists of two magnetic Hall plates used as the sensing device, a number of switches to implement the current spinning, a biasing circuit, Chopper Integrator and a Digital Output Control Circuit. This Section describes the implementation details of each block in the Cadence environment.
GENERAL DESCRIPTION

Implementation of Hall sensor in a 0.18 µm CMOS technology

Integrator read-out circuit

Sensor Plates
Switches
Bias Circuit

Digital Output Control Circuit

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The sensor structure uses two current generators nominally equal. The P-channel cascade current mirror replicates the bias current, $I_{bias}$. A second cascade mirror gives rise to the sink current.
Implementation of Hall Plate in a N-Well CMOS technology

- **Side view**
  - P+ \(>10^{18}\)
  - Nwell \(5\times10^{17}\)
  - N+ \(>10^{20}\)

- **Top view**
  - A **low doped N-well** makes the Hall plates. In order to reduce the flicker noise and surface carrier losses, a shallow highly **doped P+** conductive top layer covers the surface of the active area. The four contact regions in the N-well diffusion are **N+ highly doped**.
**Integrator Read-out Circuit**

**TABLE. PERFORMANCE SUMMARY**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.18 µm</td>
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<tr>
<td>Supply Voltage</td>
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<tr>
<td>DC GAIN</td>
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<tr>
<td>GBW</td>
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<td>Load Cap</td>
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<td>Output Range</td>
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CHIP MICROPHOTOGRAPH

Integrator Read-out
Op-amp Implementation

Sensor Plates

Switches Current Spinning
Bias Circuit
Digital Implementation

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### General Description

#### Transistor Level Implementation

Post-Layout Simulation of Differential Output Voltage Vs. Magnetic Field

<table>
<thead>
<tr>
<th>$B_z$ (mT)</th>
<th>$V_{os}$ (mV)</th>
<th>$V_{output}$ (V)</th>
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<td>-0.0024</td>
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<td>0.412</td>
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</tbody>
</table>

### Diagram

- **$V_{os}=10\text{mV}$**
- **$V_{os}=8\text{mV}$**
- **$V_{os}=5\text{mV}$**
- **$V_{os}=3\text{mV}$**
- **$V_{os}=1\text{mV}$**
- **$V_{os}=0$**

**Magnetic Field (T)**

**Differential Output Voltage (V)**

**Graph showing the relationship between magnetic field and output voltage for different $V_{os}$ levels.**
Outline

- Introduction and Motivation
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- Circuit Implementation
- Test and Measurements
- Conclusion And Future Work
The complete integrated current-mode Hall sensor system has been implemented in a 6-metal 0.18-μm CMOS technology. The system occupies only 300×200 μm^2, where only 250×150 μm^2 is for the integrator read-out circuit. Sensors and relevant switches for current spinning occupy 80×50 μm^2.
The measured differential sensor output current, $I_{\text{Hall}}$, as a function of the sensor bias current for two different magnetic field, 5 mT and 7 mT. $I_{\text{bias}}$ is ranging from 0 to 48 µA. The figure shows that the sensor has a good linearity with respect to the applied magnetic field.

The sensitivity ($S$), as a function of the sensor bias current (ranging from 6 to 48 µA) two different magnetic fields, 5 mT and 7 mT. The measured sensor sensitivity is within the 0.013 T$^{-1}$ ~ 0.02 T$^{-1}$ range.

$$S_I = \frac{I_{\text{Hall}}}{I_{\text{bias}}B}$$
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<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensitivity</td>
<td>0.02/T</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>1.8 V</td>
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<tr>
<td>Measurement Range</td>
<td>0 ~ 10 mT</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>0.013~0.02 T⁻¹</td>
</tr>
<tr>
<td>System</td>
<td>300×200 μm²</td>
</tr>
<tr>
<td>Integrator</td>
<td>250×150 μm²</td>
</tr>
<tr>
<td>Sensor and Switches</td>
<td>80×50 μm²</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>Sensor: 65 µW</td>
</tr>
<tr>
<td></td>
<td>Integrator: 54 µW</td>
</tr>
</tbody>
</table>

**Chip**

- **Technology:** 0.18-µm CMOS
- **Metal Levels:** 6
- **Area:** 300×200 μm²
- **Package:** 24-pins DIL
- **Voltage:** 1.8V
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Test and Measurements

Conclusion And Future Work
Two Hall plates operating in the current-mode and able to provide differential currents at the output nodes has been fabricated in a standard 0.18-μm CMOS process.

Measurement results show that the Hall sensor achieves a sensitivity better than $0.02 \text{ T}^{-1}$ when the magnetic field is in the range from 0 to 10 mT.

The use of the crossed-shaped Hall plates and a current-mode approach enables current spinning technique for offset cancellation.

The power consumption is in the tens of μW range considering a supply voltage of 1.8 V.
SNAPSHOT AND KEY RESULTS

FUTURE WORK

Continuing the Measurements
On Hall Sensor and Its Integrator

Integrated NMR and Hall Sensor
For Biomedical Application

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Course: TOM 2013
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Analog Integrated Circuits
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THANKS FOR YOUR ATTENTION!